Errata

Title & Document Type: **853A Economy Spectrum Analyzer Operation and Service Manual**

Manual Part Number: **00853-90010**

Revision Date: **August 1982**

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ECONOMY SPECTRUM ANALYZER OPERATION

HP Part No. 00853-90010

Printed: AUGUST 1982

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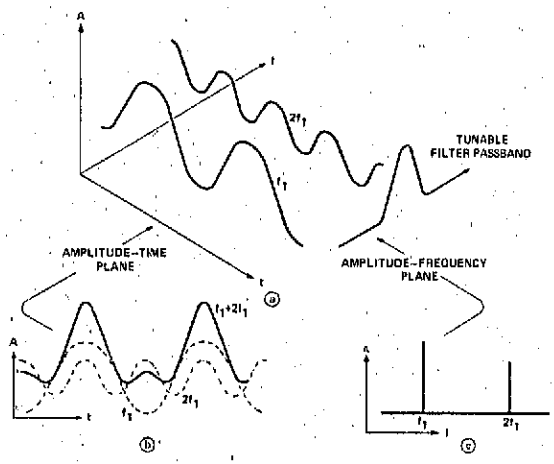
INTRODUCTION

SIGNAL ANALYSIS

The spectrum analyzer is a receiver that displays signals in the frequency domain. The CRT on the spectrum analyzer mainframe displays signal amplitude (A) on the vertical axis (see Figure 1) and frequency (f) on the horizontal axis. To visualize how a spectrum analyzer displays the frequency domain, picture a tuneable bandpass filter that scans the frequency axis. At any point on the frequency axis, the spectrum analyzer displays only the signal component it is tuned to receive, rejecting all others. In this way, the individual frequency components of a signal are viewed separately. In comparison, an oscilloscope displays the signal in the time domain, and the displayed amplitude represents the vector sum of all signal components.

This manual will acquaint you with various kinds of spectrum measurements, and the techniques for making them with a Hewlett-Packard economy spectrum analyzer: Model 8559A, 8558B, or 8557A. Further information on specific topics related to signal analysis is available in HP Application Notes, which can be obtained by contacting your nearest Hewlett-Packard sales office.

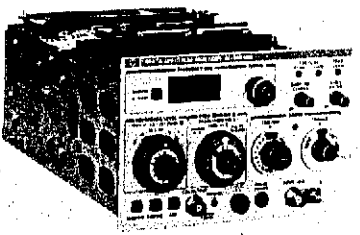


THE FREQUENCY-TIME DOMAINS

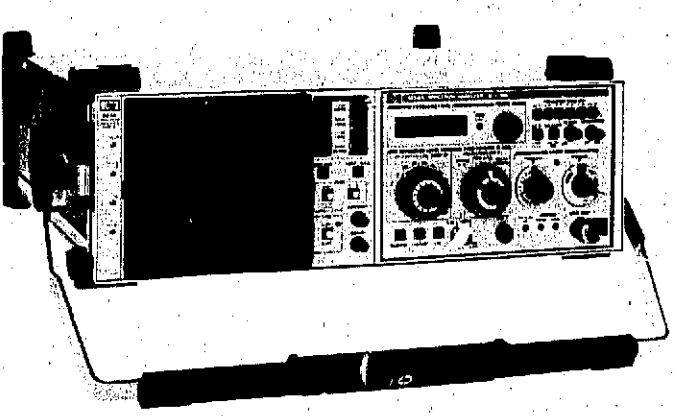
a. Three-dimensional coordinates showing time, frequency, and amplitude. The addition of a fundamental and its second harmonic is shown as an example.
b. View seen in the t-A plane. On an oscilloscope, only the composite $f_1 + 2f_1$ would be seen.
c. View seen in the f-A plane. Note how the components of the composite signal are clearly seen here.

Figure 1. Frequency and Time Domain

HP 8558B



HP 8557A



HP 853A/8559A

Figure 2. The HP Economy Spectrum Analyzer Family

BASIC DESCRIPTION

An HP economy spectrum analyzer consists of either the HP 853A Spectrum Analyzer Display mainframe or an HP 180-series Display mainframe plus one of three different spectrum analyzer plug-ins: the HP 8559A Spectrum Analyzer, the HP 8558B Spectrum Analyzer, or the HP 8557A Spectrum Analyzer. The HP 853A Display mainframe and the three plug-in spectrum analyzers are shown in Figure 2.

HP 8559A Spectrum Analyzer

The HP 8559A Spectrum Analyzer plug-in employs harmonic mixing to cover a measurement range of 10 MHz to 21 GHz in six frequency bands. It can display frequency spans as narrow as 100 kHz, and as wide as 9 GHz (the latter in full span mode). A five-digit LED readout indicates the spectrum analyzer center frequency with a resolution of 1 MHz. The HP 8559A can be used to measure signals over an amplitude range of −111 dBm to +30 dBm.

HP 8558B Spectrum Analyzer

The HP 8558B Spectrum Analyzer plug-in has a measurement range of 100 kHz to 1500 MHz, and can display frequency spans from 50 kHz to 1000 MHz. A four-digit LED readout indicates the spectrum analyzer start or center frequency with a resolution of 1 MHz or 100 kHz. The HP 8558B can be used to measure signals over an amplitude range of −117 dBm to +30 dBm. A front-panel 1ST LO OUTPUT is provided for stimulus/response measurements, using the HP 8444A Option 059 Tracking Generator.

HP 8557A Spectrum Analyzer

The HP 8557A Spectrum Analyzer plug-in has a measurement range of 10 kHz to 350 MHz, and can display frequency spans as narrow as 50 kHz, and as wide as 350 MHz. A four-digit LED readout indicates the spectrum analyzer start or center frequency with a resolution of 1 MHz or 100 kHz. The HP 8557A can measure signals over an amplitude range of −117 dBm to +20 dBm.

Features common to the three economy spectrum analyzer plug-ins include:

- Zero span mode enables operation as a manually-tuned receiver for time domain display of signal modulation.
- Resolution bandwidths in 1–3 sequence from 1 kHz to 3 MHz.
- Frequency span control and resolution bandwidth control can be coupled to function as a single "zoom" control.
- Automatic sweep control coupled to frequency span, resolution bandwidth, and video filter to maintain CRT display calibration.
- Absolute amplitude calibration and direct readout of the reference level. CW signals at or below the reference level are automatically below the gain compression level.
- Low internal harmonic and intermodulation distortion, typically provides greater than 70 dB of dynamic range for distortion measurement.
- Probe power jack for signal analysis with high-impedance active probes, such as the HP 1121A (features on HP 8558B and 8557A only).

HP 853A Spectrum Analyzer Display

The HP 853A Spectrum Analyzer Display is a large-screen, digital storage display mainframe for use exclusively with the HP 8559A, 8558B, and 8557A Spectrum Analyzer plug-ins. Digital memory provides buffer storage for two independent traces, both of which can be displayed or blanked as desired. Digital processing also provides push-button features such as maximum signal hold, digital averaging, and trace normalization. A conventional analog display mode can also be selected.

The HP 853A has limited HP-IB capabilities. CRT trace and graticule data is dumped directly to a listen-only HP-IB plotter by pressing two front-panel push buttons. Control settings on the spectrum analyzer plug-in cannot be monitored via the HP-IB; however, all digital display functions are programmable via a controller, and two lines of annotation can be displayed on the CRT for labelling purposes or operator prompting. In addition, controller commands allow transfer of trace data for analysis or storage.

CHAPTER 1
GETTING STARTED

OPERATING PRECAUTIONS

The HP 8559A, 8558B, and 8557A Spectrum Analyzer plug-ins are sensitive measuring instruments. Overloading their inputs with too much power, peak voltage, or dc voltage will permanently damage their input circuits. Do not exceed the input levels specified below:

Maximum Input (Damage) Levels

HP 8559A

Total Power:
+20 dBm (0.1W, 2.2 Vrms) with 0 dB input attenuation
+30 dBm (1W, 7.1 Vrms) with ≥10 dB input attenuation

dc or ac (<100 Hz): ±7.1V

Peak Pulse Power: +50 dBm (100W, >10 μsec pulse width, 0.01% duty cycle) with ≥30 dB input attenuation

HP 8558B

Total Power:
+30 dBm (1W, 7.1 Vrms)

dc or ac (<100 Hz): ±50V

Peak Pulse Power: +50 dBm (100W, >10 μsec pulse width, 0.01% duty cycle) with ≥20 dB input attenuation

HP 8557A

Total Power:
+20 dBm (0.1W, 2.2 Vrms)

dc or ac (<100 Hz): ±30V

NOTE

When you are measuring input signals of unknown power levels, a preliminary instrument setting of ≥30 dB INPUT ATTEN is recommended.

CAUTION

Although the spectrum analyzer's reference level can be set for power levels up to +60 dBm, the total input power must not exceed the absolute maximum limits listed above.

LINE POWER ON

Before connecting the line power cord, make sure the proper line voltage and line fuse have been selected for the display mainframe. Failure to set the ac power input selector on the display mainframe to correspond with the level of the ac source voltage could cause damage to the instrument when the power cord is plugged in.

WARNING

The spectrum analyzer and any device connected to it must be connected to power line ground. Failure to ensure proper grounding could result in a shock hazard to personnel or damage to the instrument.

LINE power is switched at the display mainframe front panel. A safety indicator lights when the ac power is on. **NEVER** remove a spectrum analyzer plug-in from the display mainframe without first switching the ac LINE power switch to OFF.

For optimum performance, you should allow the spectrum analyzer to warm up for at least 30 minutes before using it to make measurements.

FRONT-PANEL ADJUSTMENT PROCEDURE

The front-panel adjustment procedure adapts the HP 8559A, 8558B, or 8557A Spectrum Analyzer plug-in to a particular display mainframe, and should be performed daily after instrument warm-up. The step-by-step adjustment is also an excellent way for new users to become acquainted with the various spectrum analyzer controls. Once the procedure is completed, the spectrum analyzer is calibrated for absolute amplitude and frequency measurements. Make the adjustment settings shown in Table 1 before you start the adjustment procedure.

DISPLAY ADJUSTMENTS – HP 853A Spectrum Analyzer Display

1. Switch LINE power OFF then ON while holding PLOT GRAT push button depressed to activate the

Table 1. Adjustment Settings

Function	Setting
Spectrum Analyzer Plug-In	
INPUT ATTEN (dB)*	10 dB
REFERENCE LEVEL	0 dBm
Option 002	+50 dBmV
REF LEVEL FINE	0 dBm
Amplitude Scale	LIN
FREQ SPAN/DIV	10 MHz (uncoupled)
RESOLUTION BW	1 MHz (uncoupled)
SWEEP TIME/DIV	AUTO
SWEEP TRIGGER	FREE RUN
START–CENTER (8558B, 8557A)	CENTER
FREQUENCY BAND GHz (8559A)	.01–3
TUNING	>60 MHz
BASELINE CLIPPER	OFF
VIDEO FILTER	OFF
*On older plug-ins, set OPTIMUM INPUT to –30 dBm.	
HP 853A Spectrum Analyzer Display	
TRACE A	WRITE
TRACE B	STORE BLANK
DGTL AVG	OFF
INPUT–B→A	OFF
HP 180-Series Display Mainframe	
DISPLAY	INT
MAGNIFIER	X1
SCALE (180TR, 182T)	OFF
PERSISTENCE (181T/TR)	MIN
Display Mode (181T/TR)	WRITE

digital test routines. The "#0" that appears on the left side of the CRT means digital test routine #0 is now activated.

2. Press and release the PLOT GRAT push button four times to step to digital test routine #4, as indicated by the "#4" displayed on the left side of the CRT.

3. With an adjustment tool, adjust the FOCUS control as necessary to make the characters on the CRT as clear as possible.

4. Adjust the X POSN and Y POSN controls to align the square trace pattern with the outermost CRT graticule lines.

5. Momentarily press the PLOT GRAT and PLOT TRACE push buttons simultaneously to exit the digital test routines.

DISPLAY ADJUSTMENTS – HP 180-Series Display Mainframe

1. With an adjustment tool, adjust the VERTICAL POSN control to place the CRT trace on a horizontal graticule line near the CRT center.

2. Reduce the INTENSITY and set the SWEEP TIME/DIV control to MAN. Use the MAN SWEEP knob to center the CRT dot.

CAUTION

Leaving a dot on the CRT for prolonged periods at high intensity can burn the phosphor.

3. Adjust FOCUS and ASTIG controls for the smallest round dot possible.

4. Reset the SWEEP TIME/DIV control to AUTO and increase the INTENSITY for an optimum CRT trace. Adjust the HORIZONTAL POSITION control to center the CRT trace. If the horizontal deflection is not exactly 10 divisions, adjust the HORIZ GAIN control located on the rear panel of the spectrum analyzer plug-in.

NOTE

To adjust the HORIZ GAIN, you must switch the LINE power OFF, then remove the spectrum analyzer plug-in from the mainframe.

5. Adjust TRACE ALIGN so that the CRT trace is parallel to the horizontal graticule lines.

FREQUENCY AND AMPLITUDE ADJUSTMENTS — HP 8558B Spectrum Analyzer

1. Adjust VERTICAL POSN until the CRT trace aligns with the bottom CRT graticule line.

2. Connect the 35 MHz CAL OUTPUT to the spectrum analyzer input and center the 35 MHz signal with the TUNING control.

3. Narrow the FREQ SPAN/DIV to 200 kHz and adjust the REF LEVEL FINE control as necessary to position the 35 MHz signal peak near the top CRT graticule line.

4. Center the signal again, if necessary, and adjust FREQ CAL to calibrate the FREQUENCY GHz readout at 0.035 GHz.

5. Set the FREQ SPAN/DIV control to 1 MHz and adjust the REF LEVEL FINE control to place the 35 MHz signal peak at the top CRT graticule line.

6. Press the 10 dB/DIV Amplitude Scale push button. Adjust VERTICAL GAIN to place the signal peak at the top CRT graticule line.

7. Press the LIN Amplitude Scale push button. Adjust the REF LEVEL FINE control to place the signal peak at the top graticule line.

8. Repeat steps 6 and 7 until the signal peak remains at the top CRT graticule line when the Amplitude Scale is alternated between 10 dB/DIV and LIN.

9. Set the REF LEVEL FINE control to 0 and the REFERENCE LEVEL control to −10 dBm.

10. Press the LIN Amplitude Scale push button and adjust REF LEVEL CAL to place the signal peak at the top CRT graticule line.

FREQUENCY AND AMPLITUDE ADJUSTMENTS — HP 8557A Spectrum Analyzer

1. Adjust VERTICAL POSN until the CRT trace aligns with the bottom graticule line.

2. Center the LO feedthrough (i.e., the "signal" at 0 MHz) on the CRT with the TUNING control, pressing the FREQUENCY CAL push button two or three times to remove tuning hysteresis in the first LO (YIG oscillator).

3. Narrow the FREQ SPAN/DIV to 200 kHz and press the FREQUENCY CAL push button once more. Adjust the REF LEVEL FINE control as necessary to position the signal peak near the top CRT graticule line.

4. Center the LO feedthrough again, if necessary, and adjust FREQUENCY ZERO to calibrate the FREQUENCY MHz readout at 00.0 MHz.

5. Set the FREQ SPAN/DIV control to 1 MHz and the REF LEVEL FINE control to 0. Adjust the TUNING control for a FREQUENCY MHz readout of approximately 280 MHz.

6. Press the 10 dB/DIV Amplitude Scale push button, and set the REFERENCE LEVEL control to −20 dBm (+30 dBmV for Option 002 instrument).

7. Connect the 280 MHz CAL OUTPUT to the spectrum analyzer input. Center the signal on the CRT with the TUNING control, pressing the FREQUENCY CAL push button two or three times. The FREQUENCY MHz readout will indicate 280 MHz ±5 MHz.

8. Press the LIN Amplitude Scale push button. Adjust the REF LEVEL FINE control to place the signal peak at the top CRT graticule line.

9. Press the 10 dB/DIV Amplitude Scale push button. Adjust VERTICAL GAIN to place the signal peak at the top CRT graticule line.

10. Repeat steps 8 and 9 until the signal peak remains at the top CRT graticule line when the Amplitude Scale is alternated between 10 dB/DIV and LIN.

11. Set the REF LEVEL FINE control to 0, and the REFERENCE LEVEL control to −30 dBm (+20 dBmV for Option 002 instruments).

12. Press the LIN Amplitude Scale push button and adjust REF LEVEL CAL to place the signal peak at the top CRT graticule line.

FREQUENCY AND AMPLITUDE ADJUSTMENTS — HP 8559A Spectrum Analyzer

1. Adjust VERTICAL POSN to align the CRT trace with the bottom graticule line.

2. Center the LO feedthrough (i.e., the "signal" at 0 MHz) on the CRT with the TUNING control.

3. Narrow the FREQ SPAN/DIV to 200 kHz. Adjust the REF LEVEL FINE control as necessary to position the signal peak near the top CRT graticule line.

4. Center the LO feedthrough again, if necessary, and adjust FREQ ZERO to calibrate the FREQUENCY MHz readout at 00.0 MHz.

5. Set the FREQ SPAN/DIV control to 1 MHz and the REF LEVEL FINE control to 0. Adjust the TUNING control for a FREQUENCY MHz readout of approximately 250 MHz.

6. Press the 10 dB/DIV Amplitude Scale push button, and set the REFERENCE LEVEL control to −20 dBm (+30 dBmV for Option 002 instruments).

7. Connect the 250 MHz CAL OUTPUT to the spectrum analyzer input, and center the signal on the CRT with the TUNING control. The FREQUENCY MHz readout will indicate 250 MHz ±3 MHz.

8. Press the LIN Amplitude Scale push button. Adjust the REF LEVEL FINE control to place the signal peak at the top CRT graticule line.

9. Press the 10 dB/DIV Amplitude Scale push button. Adjust VERTICAL GAIN to place the signal peak at the top CRT graticule line.

10. Repeat steps 8 and 9 until the signal peak remains at the top CRT graticule line when the Amplitude Scale is alternated between 10 dB/DIV and LIN.

11. Set the REF LEVEL FINE control to 0, and the REFERENCE LEVEL control to −30 dBm (+20 dBmV for Option 002 instruments).

12. Press the LIN Amplitude Scale push button, and adjust REF LEVEL CAL to place the signal peak at the top CRT graticule line.

NORMAL SETTINGS

Certain control settings such as 10 dB/DIV, AUTO, and FREE RUN are used for the majority of measurements, and so are classified as normal settings. Table 2 lists the normal settings for the HP 8559A, 8558B, and 8557A Spectrum Analyzer plug-ins, as well as for the HP 853A Spectrum Analyzer Display and the HP 180-series Display Mainframes. Note that many of the normal settings are coded green on the front panels of the instruments.

With normal settings, most measurements are made using only the TUNING, FREQ SPAN/DIV, and REFERENCE LEVEL controls. In addition, the spectrum analyzer amplitude is calibrated for any combination of control settings as long as the AUTO sweep mode is selected. Refer to Chapter 2 for further details.

THREE-KNOB OPERATION

Most measurements made with an economy spectrum analyzer utilize only three of the spectrum analyzer controls:

TUNING adjusts the start or center frequency.

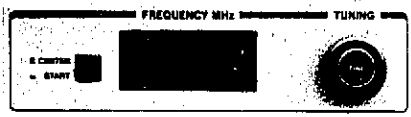
FREQUENCY SPAN/DIV selects the frequency calibration of the CRT horizontal axis. Optimum RESOLUTION BW is automatically selected whenever the two knobs are coupled with their green arrows aligned.

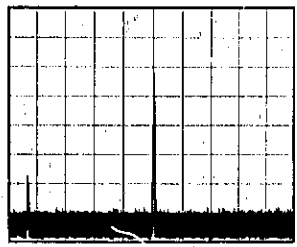
The REFERENCE LEVEL control varies the absolute power level (in dBm) at the top CRT graticule line. Changes in INPUT ATTEN also affect the reference level.

Figure 3 illustrates the use of these three controls with normal settings to make a typical measurement. The illustrations show the sequence employed to measure a signal of −20.0 dBm at 50 MHz.

Table 2. Normal Settings

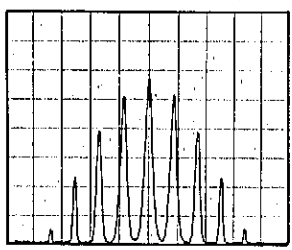
Function	Setting
Spectrum Analyzer Plug-In	
INPUT ATTEN (dB)*	10 dB
Amplitude Scale	10 dB/DIV
FREQ SPAN/DIV and RESOLUTION BW	OPTIMUM (coupled)
SWEEP TIME/DIV	AUTO
SWEEP TRIGGER	FREE RUN
START–CENTER (8558B, 8557A)	CENTER
BASELINE CLIPPER	OFF
VIDEO FILTER	OFF
ALT IF (8559A)	OFF
SIG IDENT (8559A)	OFF
*On older plug-ins, set OPTIMUM INPUT to −30 dBm.	
HP 853A Spectrum Analyzer Display	
TRACE A	WRITE
TRACE B	WRITE
DGTL AVG	OFF
INPUT–B→A	OFF
HP 180-Series Display Mainframe	
DISPLAY	INT
MAGNIFIER	X1
SCALE (180T, 180TR)	OFF
PERSISTENCE (181T/TR)	MIN
Display Mode (181T/TR)	WRITE





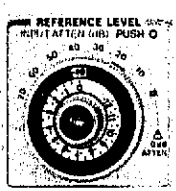
1. TUNE TO SIGNAL

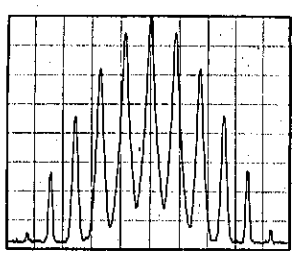
Select a wide frequency span and tune the signal to center screen with the TUNING control. Signal frequency is indicated by the FREQUENCY MHz readout (50 MHz).



2. ZOOM-IN

Reduce the frequency span. Resolution bandwidth, sweep time, and video filter bandwidth are automatically set to maintain an amplitude-calibrated display. The TUNING control can be used to adjust center frequency.





3. SET AMPLITUDE LEVEL

Raise the signal to the reference level, the top CRT graticule line, and read the amplitude in dBm (–20 dBm). The calibrated 10-dB steps and 12-dB vernier of the REFERENCE LEVEL control allow accurate IF substitution measurement of various signal amplitudes.

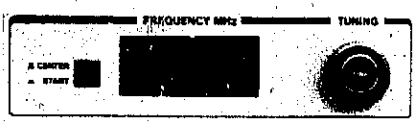
Figure 3. Measuring a Signal with an Economy Spectrum Analyzer (HP 8558B)

CHAPTER 2
FRONT PANEL OPERATION

This chapter provides detailed functional descriptions of the major front-panel controls on the HP 8559A, 8558B, and 8557A Spectrum Analyzer plug-ins, and the HP 853A Spectrum Analyzer Display mainframe. Spectrum analyzer controls are the same for all three plug-ins unless otherwise noted. All controls, indicators, and connectors on the plug-ins and on the HP 853A Display are identified and briefly described in **Appendix D, Economy Spectrum Analyzer Family Front- and Rear-Panel Features.**

HP 8559A, 8558B, and 8557A Spectrum Analyzers

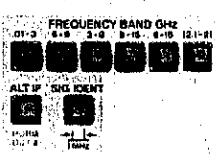
TUNING
FREQUENCY GHz (HP 8559A)
FREQUENCY MHz (HP 8558B, 8557A)
START-CENTER



The TUNING control adjusts the center frequency (or start frequency) of the spectrum analyzer. This frequency is displayed on the FREQUENCY GHz or FREQUENCY MHz readout. In addition, the TUNING control positions the tuning marker when the spectrum analyzer is being operated in the F span mode.

The START-CENTER push button selects the tuning mode of the spectrum analyzer; for example, with START selected, the FREQUENCY readout corresponds to the frequency at the left side of the CRT display. The START-CENTER push button has no effect in zero span mode because the spectrum analyzer is tuned to a fixed frequency instead of being swept.

FREQUENCY BAND GHz (HP 8559A)
SIG IDENT (HP 8559A)
ALT IF (HP 8559A)



The FREQUENCY BAND GHz push buttons on the HP 8559A perform several functions associated with harmonic mixing (refer to Chapter 3). Selection of a particular frequency band automatically shifts the FREQUENCY GHz readout and adjusts the CRT frequency and amplitude calibration as necessary for proper display of in-band signals. In addition, the input mixer is biased to provide maximum conversion efficiency for the particular LO harmonic used.

The FREQUENCY BAND GHz and SIG IDENT controls are used together to determine the harmonic mixing mode (and, therefore, the correct frequency band) for an unknown signal. On alternate sweeps, the signal identifier shifts the spectrum analyzer IF and decreases the overall gain by approximately 6 dB. When the correct frequency band is selected, the unknown signal shifts to the left by 1 MHz as shown in Figure 4. Once the unknown signal is tuned to the CRT center and is correctly identified, its frequency can be read directly on the FREQUENCY GHz readout.

The ALT IF control shifts the first IF 15 MHz to eliminate baseline lift caused by a 3 GHz input signal (normal IF is approximately 3.0075 GHz).

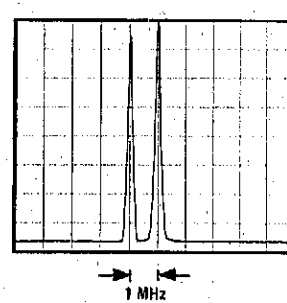
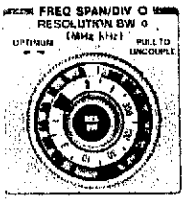


Figure 4. Correct Signal Identification with the HP 8559A

FREQUENCY CAL (HP 8558B)

The FREQUENCY CAL push button removes tuning hysteresis in the swept first LO (a YIG oscillator) of the HP 8558B. Tuning changes of more than 50 MHz should be followed by a press or two of this push button to ensure frequency accuracy; it is good practice to always press FREQUENCY CAL before calibrating the FREQUENCY MHz readout, selecting narrow spans, and making frequency measurements.

FREQUENCY SPAN/DIVISION RESOLUTION BANDWIDTH



The FREQ SPAN/DIV control sets the horizontal calibration of the CRT.

When it is pushed in, the FREQ SPAN/DIV control mechanically couples with the RESOLUTION BW control. For normal operations, the two controls are coupled with their OPTIMUM markings (><) aligned to form an effective "zoom" control.

F (Full Band – HP 8559A)

The HP 8559A sweeps the entire selected frequency band in the full-band mode. In addition, a tuning marker is displayed on the CRT, and the frequency of an in-band signal located at the tuning marker is indicated on the FREQUENCY GHz readout. Once the tuning marker is positioned under an unknown signal, the frequency span can be narrowed for detailed signal analysis. Note that displayed signals are not necessarily in the selected frequency band – the signal identifier is provided to identify the correct frequency band for an unknown signal.

F (Full Span – HP 8557A)

The HP 8557A sweeps its entire frequency range in the full span mode. The FREQUENCY MHz readout shows the frequency of the tuning marker displayed on the CRT. After the tuning marker is positioned under an unknown signal, the frequency span can be narrowed for detailed signal analysis.

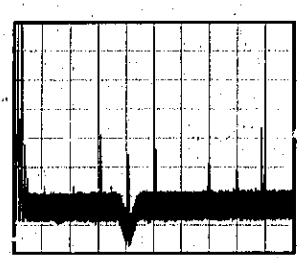


Figure 5. Tuning Marker in Full Span

MHz/DIV
kHz/DIV

The per-division mode selects a particular frequency calibration for the CRT horizontal axis. Settings are provided in a 1-2-5 sequence for a wide range of frequency spans.

0 (Zero Span)

The zero span mode can be used to recover the modulation on a carrier signal. In this mode, the first LO is tuned to a fixed frequency; and the spectrum analyzer operates as a manually tuned, variable bandwidth receiver at the frequency indicated by the FREQUENCY GHz or FREQUENCY MHz readout. This allows the carrier modulation to be displayed in the time domain, as shown in Figure 6. The calibrated SWEEP TIME/DIV control provides calibrated sweep times for use with zero span. VIDEO TRIGGER synchronizes the sweep with the demodulated waveform.

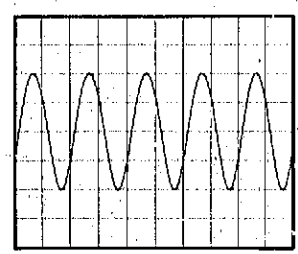


Figure 6. Time-Domain Display of a Demodulated AM Signal in Zero Span

The RESOLUTION BW control selects the spectrum analyzer 3-dB bandwidth. Eight bandwidths are provided, ranging from 1 kHz to 3 MHz in a 1-3 sequence. In normal operation, the RESOLUTION BW control is coupled with the FREQ SPAN/DIV control, and the OPTIMUM markings (> <) on the two controls are aligned to provide an aspect ratio (ratio of total span to resolution bandwidth) of approximately 1 percent. The controls may be coupled for other ratios.

Resolution bandwidth determines the sensitivity and resolution of the spectrum analyzer. Each decade of reduction in resolution bandwidths lowers the spectrum analyzer noise floor by approximately 10 dB, allowing lower signals to be measured. Additionally, a narrow resolution bandwidth enables closely-spaced signals to be resolved, as shown in Figure 7. These advantages must be balanced against the increased sweep time necessary to ensure amplitude calibration with narrower bandwidths. With the AUTO sweep time setting selected, the spectrum analyzer automatically adjusts the sweep speed to maintain a calibrated display.

REFERENCE LEVEL INPUT ATTEN, Amplitude Scale

The reference level — that is, the top CRT graticule line — is used to make accurate amplitude measurements. The reference level is determined by a combination of IF gain (REFERENCE LEVEL control) and RF attenuation (INPUT ATTEN control). The REFERENCE LEVEL/INPUT ATTEN control knob adjusts the IF gain in 10-dB steps, and when pushed in, adjusts the input attenuation. The FINE control is a calibrated vernier which provides 12-dB of continuous IF gain adjustment.

Input attenuation (blue numbers) can be adjusted in 10-dB steps by pushing and turning the outer REFERENCE LEVEL knob. Except for noise measurements, or when maximum sensitivity is required, a minimum INPUT ATTEN setting of 10 dB is recommended to ensure good input SWR and amplitude accuracy.

The REFERENCE LEVEL/INPUT ATTEN control may be used to make both relative and absolute measurements. Of the two methods, absolute amplitude measurement provides the greater accuracy and is recommended especially for measuring low-level signals.

To make an absolute amplitude measurement, position the peak of the input signal on the reference level line with the REFERENCE LEVEL control. In the example shown in Figure 8, the amplitude of f1 is −10 dBm.

To make a relative amplitude measurement, use the REFERENCE LEVEL control and the 10 dB/DIV and 1 dB/DIV Amplitude Scale push buttons. In Figure 8, the amplitude of f2 can be read from the CRT display as −60 dBm; that is, 50 dB below the reference level of −10 dBm. Note that with an Amplitude Scale of 10 dB/DIV selected, the CRT is calibrated over the top seven divisions, with the bottom division compressed for ease in locating low-level signals.

Pressing the LIN push button selects an Amplitude Scale proportional to volts, with the bottom graticule line representing 0 volts and the top graticule line (the reference level) unchanged.

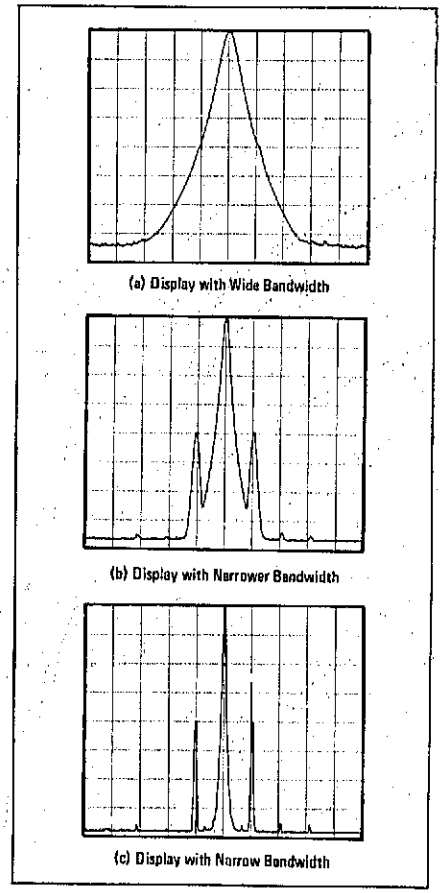


Figure 7. Narrowing of the IF Filters Allows Resolution of Adjacent Signals

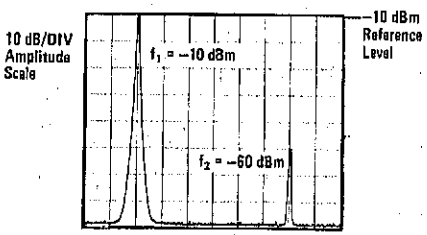
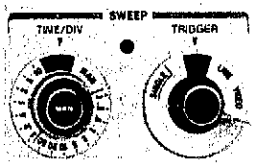


Figure 8. Relative and Absolute Amplitude Measurements

SWEEP TIME/DIV
SWEEP TRIGGER



The SWEEP TIME/DIV control selects the sweep speed of the spectrum analyzer in much the same way as its oscilloscope counterpart. The Per-Division mode permits manual selection of a calibrated sweep time, which is useful for making time-domain measurements in zero span. Sweep time can be manually selected with other frequency span settings as well (such as MHz/DIV, kHz/DIV, etc); however, the sweep speed **must** be slow enough to allow the spectrum analyzer to fully respond to input signals. If the spectrum analyzer is being swept too fast for the selected settings, signal responses will droop, yielding incorrect amplitude readings.

The AUTO mode is recommended for normal operation. When SWEEP TIME/DIV is set to AUTO, the sweep time is automatically adjusted for all FREQUENCY SPAN/DIV, RESOLUTION BW, and VIDEO FILTER control settings to maintain a calibrated amplitude display. The effect of the AUTO SWEEP setting can be observed by decreasing the video filter bandwidth. The sweep rate slows automatically with narrower video filter bandwidths to allow the spectrum analyzer more time to respond. A similar effect results when the resolution bandwidth is narrowed, or the frequency span is widened.

The MAN (manual) mode enables you to sweep the spectrum analyzer across the frequency band with the MAN SWEEP control.

The SWEEP TRIGGER control provides four different modes for triggering the spectrum analyzer sweep. LINE, FREE RUN, and SINGLE operate in much the same manner as their oscilloscope counterparts. The spring-loaded SINGLE SWEEP setting stops or starts the sweep.

The VIDEO TRIGGER setting allows the spectrum analyzer to be triggered on a detected modulation waveform. Approximately one-half major division of amplitude change, as seen on the CRT, is necessary to trigger a sweep. Video triggering in zero span mode allows accurate time-domain measurements of many modulation waveforms, without the need for a specialized receiver.

VIDEO FILTER

The VIDEO FILTER control is useful for noise measurements and observations of low-level signals close to the spectrum analyzer noise floor. The video filter is a post-detection low-pass filter which smooths the CRT trace by averaging random noise, as shown in Figure 9. The video filter bandwidth is automatically scaled to the RESOLUTION BW setting. The MAX (detent) position selects a 1.5 Hz video filter bandwidth for maximum noise averaging. This position is provided for noise-level and sensitivity measurements, and should **not** be used for measurements of CW signals.

BASELINE CLIPPER

The BASELINE CLIPPER control is used to prevent baseline "blooming" when the spectrum analyzer is operated in an HP 181T/TR Display mainframe. The baseline clipper blanks a variable lower portion of the CRT display. The control has no effect when an HP 853A Spectrum Analyzer Display mainframe is being used, except in the analog display mode.

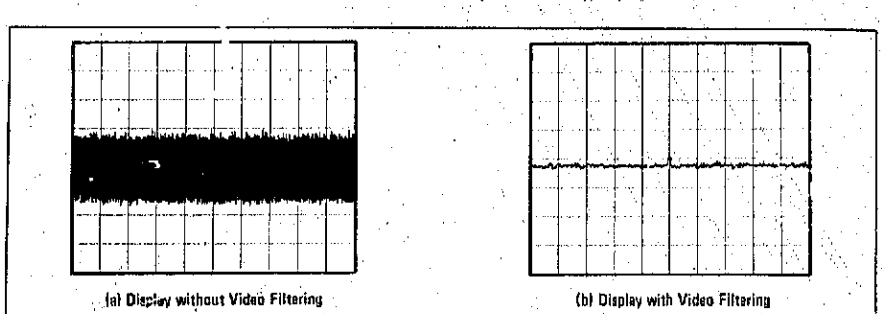


Figure 9. Video Filtering

HP 853A Spectrum Analyzer Display

TRACE A
TRACE B

Two digital trace memories (A and B) are provided for independent storage of two CRT traces. The video signal from the spectrum analyzer plug-in is converted to digital information and stored in trace memory (see Figure 10). The trace memory is in turn written to the CRT display at a refresh rate of about 55 Hz (rapid enough to prevent trace flickering). Trace A and trace B may be displayed separately or simultaneously.

CLEAR WRITE

In the clear write mode, the trace memory is continuously updated with the current input signal data, and the contents of trace memory are displayed on the CRT.

MAX HOLD

In the maximum hold mode, the contents of the trace memory are continuously compared with the current input signal data and are updated to reflect the maximum signal values. The contents of trace memory are displayed on the CRT.

STORE VIEW

In the store view mode, the data currently in the trace memory are preserved and displayed on the CRT.

STORE BLANK

In the store blank mode, the data currently in the trace memory are preserved but are not displayed on the CRT.

ANALOG DISPLAY

The analog display mode is selected by pressing both STORE BLANK push buttons. In this mode, the CRT display switches to a conventional analog display of the current input signal.

DGTL AVG

Digital averaging improves the ability of the spectrum analyzer to measure low-level signals – signals that might otherwise be masked by noise. Unlike video filtering, digital averaging smooths the CRT trace without necessitating an increase in spectrum analyzer sweep time.

To use digital averaging, first select the spectrum analyzer control settings for the measurement you wish to perform. Then press the DGTL AVG push button and note the reduction in displayed noise on the CRT. Digital averaging should be restarted after any change you make in the spectrum analyzer control settings to ensure that all signals are displayed with the proper amplitude calibration.

Digital averaging employs a filtering algorithm that averages trace data from sweep to sweep. After the initial sweep, the trace data for each subsequent sweep is exponentially weighted and added to the contents of the trace memory. Thus, the degree of trace averaging is directly related to the number of sweeps. The exponentially weighted algorithm is expressed as follows:

$$Y_N = S_N \qquad (N = 1)$$

$$= Y_{N-1} + (S_N - Y_{N-1})/F \qquad (1 < N < 64)$$

$$= Y_{N-1} + (S_N - Y_{N-1})/64 \qquad (N > 64)$$

Where Y_N = current contents of trace memory

Y_{N-1} = previous contents of trace memory

S_N = current input signal data

N = sweep number

$F = 2^{[\mathrm{INT}(\log_2(N))]}$

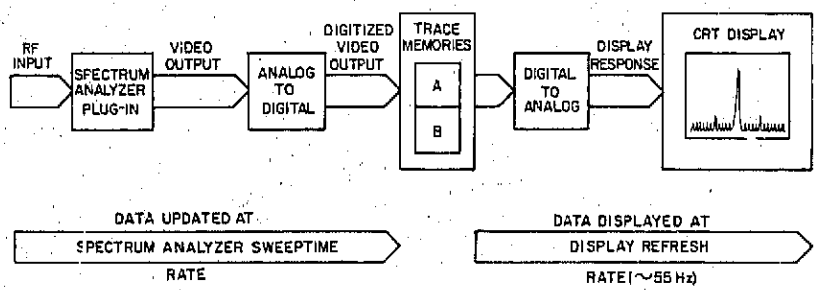


Figure 10. Trace Memory in the HP 853A Spectrum Analyzer Display

In other words, the difference between the previous average and the current input signal is divided by F. The result is then added to the previous average to obtain the new average. F increases from 2 to a fixed value of 64 so that maximum digital averaging is quickly approached with a minimum number of sweeps.

INPUT - B→A

The trace arithmetic feature of the HP 853A can be used for either comparison of two traces or trace normalization during swept-frequency measurements. Trace normalization corrects for minor deviations in the frequency response characteristics (flatness) of a measurement system.

When INPUT - B→A is selected, the contents of the trace B memory are subtracted point-by-point from the current input signal data before the input signal data is stored in the trace A memory. Trace B must, therefore, be in one of the store modes during trace arithmetic. If the current input signal data are identical to the contents of the trace B memory, a straight horizontal trace (reference trace) will be stored in the trace A memory.

The location of the reference trace during trace arithmetic has been preset at the factory to midscreen on the CRT. A small jumper connection, inside the HP 853A on Processor Assembly A7, allows the reference trace location to be moved to top-screen or midscreen (see Figure 11).

WARNING

Positioning of the trace arithmetic jumper on Processor Assembly A7 can only be accomplished with the HP 853A bottom cover removed. Since this exposes a number of high-voltage points, the work should be done only by a qualified service technician who is aware of the hazard involved. To avoid the possibility of electrical shock, the HP 853A power cable should be disconnected before the bottom cover is removed.

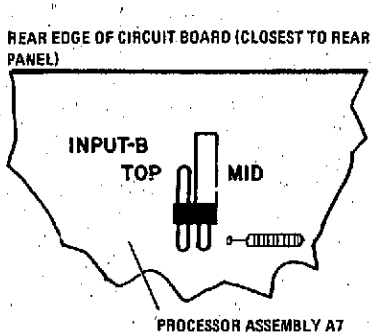


Figure 11. Trace Arithmetic Jumper

PLOT GRAT
PLOT TRACE
HP-IB CLEAR

The HP 853A PLOT push buttons allow graticule and trace information to be output directly to a digital plotter through an HP-IB cable, without the need for a controller.

NOTE

If an HP-IB controller is connected to the HP-IB connector of the HP 853A, place the controller in the reset state (i.e., terminate any running program) before the direct plot routine is executed.

Digital plotters can provide full-size copies – up to 11 by 16 inches (approximately 279 by 406 mm) with the HP 9872C – that are ideal for laboratory reports, and which can be reproduced more easily than photographs.

The HP 7470A, HP 7225B, and the HP 9872C are among the plotters that feature HP-IB compatibility and, therefore, are directly compatible with the HP 853A. (Most of the CRT plots shown in this manual were directly plotted with the HP 7225B).

To generate a plot:

1. Attach HP-IB cable between the HP-IB connector on the rear panel of the HP 853A and the HP-IB connector on the rear panel of the plotter, as shown in Figure 12. Set the plotter to Listen-only mode.

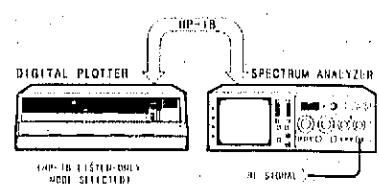


Figure 12. Digital Plotter Setup

2. Establish the lower-left and upper–right limits on the plotter. These limits will set the corner points of the graticule plot.

3. Press and release the PLOT GRAT push button to plot the graticule pattern.

4. Press and release the PLOT TRACE push button to plot the trace data displayed on the CRT.

A plot in progress may be stopped by holding down the PLOT GRAT push button for approximately three seconds to execute an HP-IB clear. This procedure can also be used to return the HP 853A from HP-IB control to local control, and to clear HP-IB error messages or labels from the CRT.

Several special test routines are built into the HP 853A to serve as adjustment aids and troubleshooting tools. These routines can be activated by first switching the LINE power ON while holding the PLOT GRAT push button pressed, then repeatedly pressing PLOT GRAT to step to the desired routine (test routine numbers are displayed on the left side of the CRT). Test routine #4 is recommended for adjustment of the TRACE ALIGN, FOCUS, X-POSN, and Y-POSN controls. Refer to Section V of the HP 853A Operation and Service Manual for further details.

CHAPTER 3
SPECIAL TOPICS

MAXIMUM DYNAMIC RANGE

The maximum dynamic range of a spectrum analyzer is defined as the maximum measurable amplitude difference (in dB) between two signals simultaneously present at the input. Depending on the particular measurement, dynamic range is limited by a combination of spectrum analyzer sensitivity, internal distortion, and gain compression. Judicious adjustment of the signal level reaching the input mixer (through the use of RF input attenuation) provides maximum dynamic range for a wide variety of spectrum analyzer measurements.

Sensitivity

Spectrum analyzer sensitivity is defined traditionally as the average noise level ("noise floor") displayed on the analyzer when no input signals are applied. It establishes an effective lower limit on the range of signal levels that can be measured. An input signal level equal to the average noise level, considered a minimum discernible signal, causes a peak approximately 3-dB above the noise. Spectrum analyzer sensitivity is dependent on the resolution bandwidth and on the frequency band selected. Internally generated noise is more or less evenly distributed in frequency (white); therefore, for every decade increase (decrease) in resolution bandwidth, the average noise level increases (decreases) by approximately 10 dB.

The HP 8559A uses harmonic mixing (harmonics of the first local oscillator) to provide calibrated operation to 21 GHz in six overlapping frequency bands. Higher harmonic mixing modes (corresponding to wider frequency bands) have higher average noise levels, due to lower conversion efficiencies in the input mixer. Therefore, best sensitivity is achieved by selecting the narrowest frequency band covering the frequencies of interest.

Mixer Level

The Mixer Level is defined as the signal level at the spectrum analyzer input minus the INPUT ATTEN setting:

MIXER LEVEL = INPUT SIGNAL − INPUT ATTEN

In other words, the mixer level reflects the signal level reaching the spectrum analyzer input mixer. (This definition is for convenience – for example, a 3-dB attenuator is located between the input attenuator and input mixer in the HP 8553L, but is not included when figuring Mixer Level.)

Gain Compression and Maximum Input (Damage) Levels

Gain compression occurs in a spectrum analyzer as the mixer level is increased above normal levels. For example, a top-screen signal for the HP 8559A corresponds to at most a mixer level of −10 dBm, ensuring less than 0.5 dB of amplitude error due to gain compression. Higher mixer levels drive the signal response off the top of the CRT and cause amplitude errors in other low-level signals. When this occurs, additional input attenuation should be used to decrease the mixer level. Note, however, that the specified maximum input level for a spectrum analyzer must never be exceeded.

Internal Distortion

Distortion products are generated in the spectrum analyzer input mixer whenever one or more signals are present, since it is a nonlinear device. Furthermore, the amplitudes of these products change nonlinearly with a change in signal amplitude. For example, a 10 dB increase in signal amplitude causes a 20 dB increase in second-order harmonics and a 30 dB increase in third-order distortion products generated in the first mixer (both approximate). For most input signals, internal distortion is negligible, being well below the displayed noise floor. RF input attenuation is used with large input signals to reduce the mixer level, lowering mixer distortion products to the noise floor for maximum dynamic range.

RF input attenuation can be used in a simple test to check whether internally generated distortion is affecting a distortion measurement. Increase the spectrum analyzer input attenuation by 10 dB while observing the CRT. Displayed signals affected by internal distortion will decrease by more than 10 dB, while true input signals will decrease by exactly 10 dB. Input attenuation can be increased as necessary to reduce internal distortion until it no longer affects the measurement at hand.

Internal distortion does not interfere with many spectrum analyzer measurements. In these cases, dynamic range is limited only by the spectrum analyzer sensitivity and gain compression level. Thus, maximum dynamic range (MDR) varies with the type of measurement to be made.

Dynamic Range Graph

The Dynamic Range Graph is a useful tool for achieving MDR for a particular spectrum analyzer measurement. Figures 13, 14, and 15 are the dynamic range graphs for the standard HP 8559A, HP 8558B, and HP 8557A, respectively.

Three types of curves are presented on a dynamic range graph: sensitivity (solid line), second-order distortion (dashed line), and third-order distortion (short-dashed line). These three curves are plotted versus mixer level, measured in dBm. Sensitivity curves are given for a 1 kHz resolution bandwidth; when using other resolution bandwidths, simply shift the appropriate sensitivity curve upwards by 10 dB (a straightedge works nicely) for each decade increase in resolution bandwidth. For example, a sensitivity curve shifts upward on the dynamic range graph by 20 dB for a 100 kHz resolution bandwidth.

Two vertical axes are used on a dynamic range graph: Signal-to-Noise Ratio (right side) and Spurious-Free Dynamic Range (left side). MDR occurs at the intersection of the particular sensitivity curve and distortion curve under consideration. This point is achieved on the spectrum analyzer by adjusting the RF input attenuation for optimum signal level at the input mixer.

Dynamic range varies as a function of mixer level. For example, a mixer level of approximately −40 dBm achieves MDR for measuring second-order distortion products with an HP 8559A (0.01 – 3 GHz). Internal second-order distortion products increase 20 dB for every 10 dB increase above this mixer level. For third-order distortion measurements, the mixer level should be approximately −33 dBm. Internal third-order distortion products increase 30 dB for every 10 dB increase above this level.

EXAMPLE. (See Figure 13.) The second-order harmonic distortion of a device is to be measured with an HP 8559A. The signal at the spectrum analyzer input has a fundamental frequency of 1146 MHz at 0 dBm (1 mW) with associated low-level distortion. Find the mixer level to achieve maximum dynamic range for the measurement.

SOLUTION. The mixer level for MDR is −40 dBm. Since this is a second-order measurement, use the dashed second-order distortion curve. Intersect this curve with the 0.01 – 3 GHz sensitivity curve, since the second-order harmonic frequency of 2292 MHz falls in this band. The MDR and optimum mixer level for a 1 kHz resolution bandwidth occurs at the intersection of the curves. The INPUT ATTEN control must, therefore, be set to 40 dB (for a mixer level of −40 dBm) to achieve an MDR of 70 dB. (See Figure 13a.)

EXAMPLE. A device is to be adjusted for minimum third-order intermodulation distortion. During testing, the device output includes two fundamental −6 dBm signals at 1146 MHz and 1156 MHz, with associated low-level distortion. Find the mixer level for the HP 8559A that will achieve maximum dynamic range for the measurement.

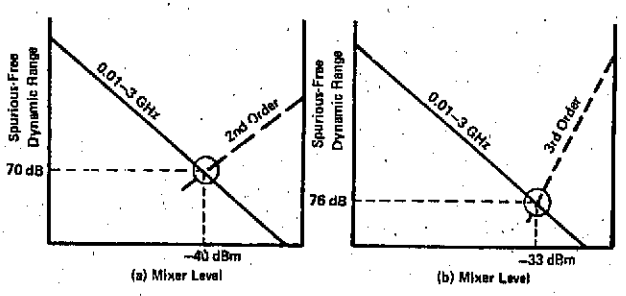
SOLUTION. The mixer level for MDR is approximately −33 dBm (−36 dBm for each fundamental). Since this is a third-order measurement, use the dotted third-order distortion curve. Intersect this curve with the 0.01 – 3 GHz sensitivity curve, since the critical third-order distortion products fall in this band. The MDR and optimum mixer level for a 1 kHz resolution bandwidths occurs at the intersection of the curves. Since the input signal level is approximately −3 dBm, the INPUT ATTEN control must be set to 30 dB (for a mixer level of −33 dBm) to achieve an MDR of 76 dB.

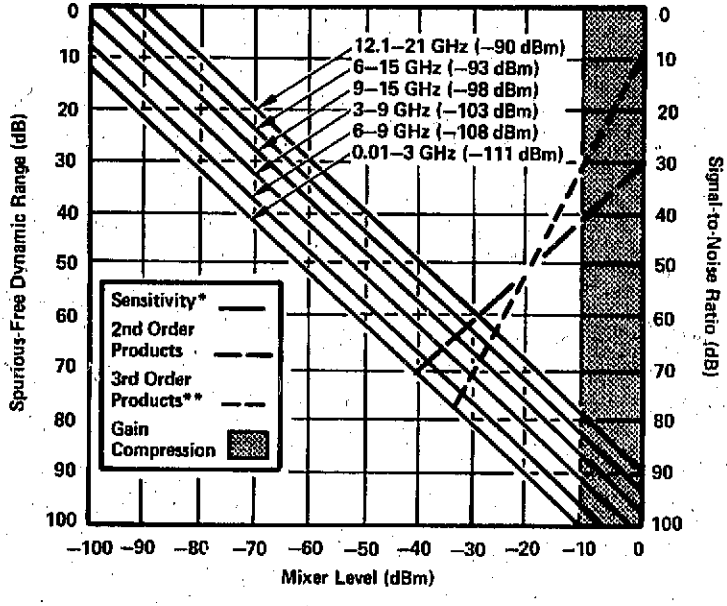
Signal-to-Noise Ratio

In many spectrum analyzer applications, internal distortion products are of little or no concern, since they do not interfere with the measurement being made. Likewise, when measuring low-level signals (≤ −40 dBm), internal distortion products are well below the spectrum analyzer noise level. In either case, dynamic range is limited only by the analyzer sensitivity (and gain compression level) and can be expressed as a signal-to-noise ratio. Simply find the mixer level on the dynamic range graph (Figure 13, 14, or 15) and go vertically to the appropriate sensitivity curve. The maximum obtainable dynamic range is read from the Signal-to-Noise Ratio (vertical) axis. Note that when measuring low-level signals (0 dB INPUT ATTEN assumed), the input signal level is equal to the mixer level and can be used directly to determine the signal-to-noise ratio.

HARMONIC MIXING

The HP 8559A Spectrum Analyzer uses harmonic mixing to cover the 0.01 – 21 GHz frequency range. While harmonic mixing makes such broad frequency coverage possible, it also allows multiple responses, image responses,

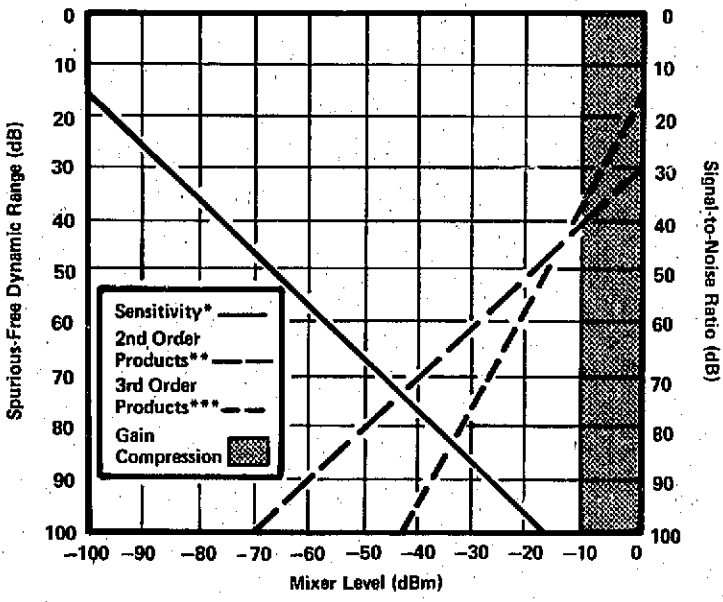




*Graph shows spectrum analyzer sensitivity for a resolution bandwidth of 1 kHz.

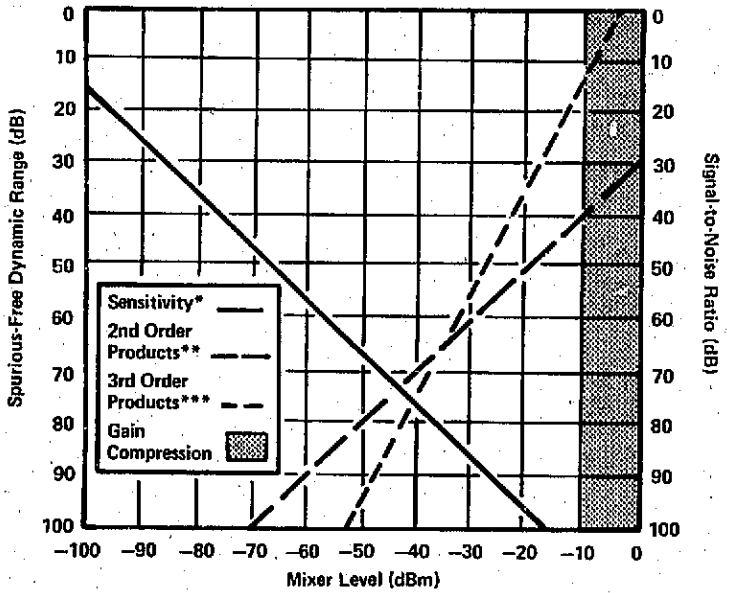
**Graph shows third order products for two equal input signals separated by 50 kHz or more.

Figure 13. Dynamic Range Graph for HP 8559A



*Graph shows spectrum analyzer sensitivity to signals ≥1 MHz, using a resolution bandwidth of 1 kHz (−117 dBm).
**Graph shows second order products for input signals ≥5 MHz.
***Graph shows third order products for two equal input signals ≥5 MHz and separated by 50 kHz or more.

Figure 14. Dynamic Range Graph for HP 8558B (Standard)



*Graph shows spectrum analyzer sensitivity to signals ≥1 MHz, using a resolution bandwidth of 1 kHz (−117 dBm).
**Graph shows second order products for input signals ≥1 MHz.
***Graph shows third order products for two equal input signals ≥1 MHz and separated by 50 kHz or more.

Figure 15. Dynamic Range Graph for HP 8557A (Standard)

and IF feedthrough. The ALT IF and SIG IDENT features of the HP 8559A provide convenient solutions to these problems and require only a basic understanding of harmonic mixing and the spectrum analyzer input section.

The block diagram in Figure 16 shows the basic input section of the HP 8559A. A 3–6 GHz local oscillator (f_{LO}) provides tuning for the spectrum analyzer. Harmonics of this frequency (nf_{LO}) are generated in the input mixer by the nonlinear mixer diode. An input signal (f_s) passes through the variable input attenuator and mixes with the LO and its harmonics, generating sum and difference signals. A response appears on the spectrum analyzer display whenever one of these mixing products falls within the bandpass of the IF section (f_{IF}). Thus, a displayed signal satisfies the equation:

$$f_s = nf_{LO} \pm f_{IF} (n = 1, 2, 3, \ldots)$$

This is the general tuning equation for a harmonic mixing spectrum analyzer. The input signal can mix with the fundamental or any of the harmonics of the LO to produce the proper IF.

Tuning Curves

The tuning equation is often graphed to help visualize the harmonic mixing process. A separate tuning curve results from each combination of sign and harmonic number n. In Figure 17, tuning curves are shown for fundamental, second harmonic, and third harmonic mixing (n = 1, 2, 3) based on an IF of 3 GHz and a 3–6 GHz LO–the approximate values used in the HP 8559A.

For example, if n = 1, the input mixes with the LO (fundamental mixing). The dotted line in Figure 17 represents the LO as it is tuned over its 3–6 GHz range. We can draw one curve using the minus sign in the equation and another for the plus sign. These represent input signal frequencies for the 1– and 1+ mixing modes, respectively. The number indicates the harmonic of the LO which is being used, and the plus or minus sign indicates the sign used in the tuning equation.

From the basic tuning equation it follows that each LO harmonic will generate a pair of parallel curves separated by twice the IF frequency (2 x 3 GHz = 6 GHz). Thus, the first three harmonics of the LO provide six frequency bands (or harmonic mixing modes), each with a frequency span equal to that of the LO (3 GHz) multiplied by the particular harmonic number used. For example, the 6–15 GHz frequency band uses the 3– harmonic mixing mode and spans 9 GHz. These six bands allow calibrated measurement of input signals up to 21 GHz.

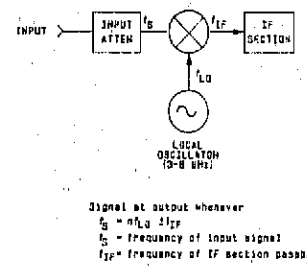


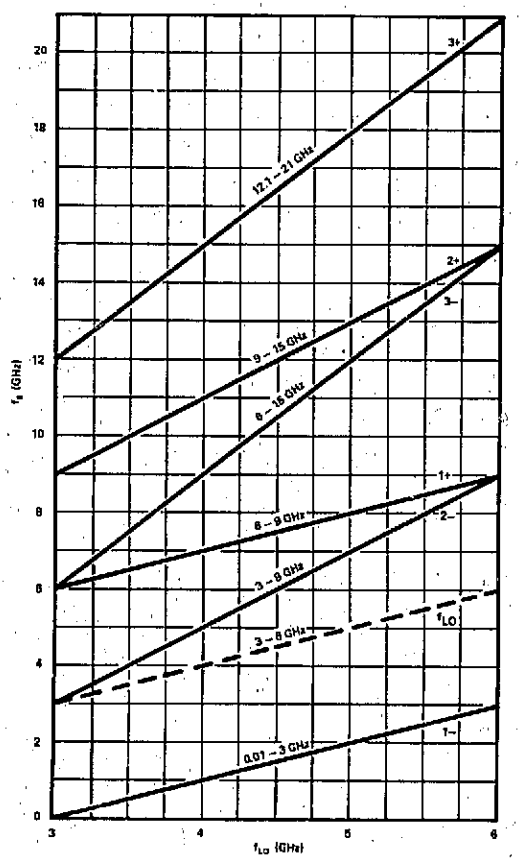
Figure 16. HP 8559A Simplified Input Block Diagram

The HP 8559A front panel lists the nominal frequency limits for each frequency band. Table 3 lists the specified frequency band limits and corresponding harmonic mixing modes. Note that use of the ALT IF feature changes the lowest specified frequency for each band.

Table 3. HP 8559A Specified Frequency Band Limits

Frequency Band GHz (nominal)	Harmonic Mixing Mode	Lowest Frequency (GHz) [ALT IF]	Highest Frequency (GHz)
.01–3	1–	0.010 [0.025]	3.060
6–9	1+	6.035 [6.020]	9.060
3–9	2–	3.033 [3.048]	9.120
9–15	2+	9.058 [9.043]	15.120
6–15	3–	6.055 [6.070]	15.180
12.1–21	3+	12.080 [12.065]	21.000

The six Frequency Band GHz buttons on the HP 8559A perform several functions associated with harmonic mixing. Selection of a particular frequency band automatically scales and shifts the Frequency GHz display to the correct center frequency. The input mixer is biased to provide maximum conversion efficiency for the particular LO harmonic used. Additionally, the LO sweep range and internal gains are adjusted, calibrating the display for all in-band input signals.



$f_S = nf_{LO} \pm f_{IF}$

$f_{IF} \approx 3.0075$ GHz (normal)

≈ 2.9925 GHz (ALT IF)

Figure 17. HP 8559A Tuning Curves

Image Responses

A harmonic mixing spectrum analyzer such as the HP 8559A sweeps all of its frequency bands simultaneously. Thus, a response on the CRT corresponds to one of several possible input signal frequencies. For example, input signals near 1 GHz and 7 GHz can both mix with 4 GHz from the LO to produce the IF frequency of 3 GHz. Similar image pairs can occur for each LO harmonic. Figure 18 illustrates six possible image responses for a 4 GHz LO frequency.

Multiple Responses

Multiple responses to a single input signal are also possible with a harmonic mixing spectrum analyzer because of overlapping of the different frequency bands. For example, Figure 19 illustrates that an HP 8559A with a 7 GHz input signal will display as many as three distinct signal responses, corresponding to three possible harmonic mixing modes.

Signal Identifier

The SIG IDENT feature of the HP 8559A is used to verify the mixing mode of unknown signals for proper frequency band selection. On every other sweep, the signal identifier shifts the IF frequency (2nd LO) 1 MHz higher and lowers the entire CRT trace approximately 3 minor divisions. A signal shifts 1 MHz to the left on the CRT display (and drops in amplitude) only when the correct frequency band is selected, as shown in Figure 4. The unknown signal can then be tuned to the CRT center to read its frequency directly on the FREQUENCY GHz readout.

Multiple and image responses are easily identified with the signal identifier. When image responses are present, they appear as a single response on the CRT. The signal identifier separates the images, since each harmonic mixing mode exhibits a different shift. ALT IF or simple bandpass filtering prevents images from interfering with the analysis of the desired signal.

IF Feedthrough and ALT IF

On occasion, an input signal may be present that falls within the IF passband of the HP 8559A (approximately 3 GHz). This signal can pass directly through the input mixer, causing baseline lift – a rise in the "noise floor" on the spectrum analyzer display.

The ALT IF feature of the HP 8559A shifts both the LO and IF frequencies by 15 MHz to provide an alternate IF frequency without the necessity of retuning. Switching to the alternate IF allows measurements in the presence of input signals that would normally cause baseline lift. In addition, image responses are separated, since each out-of-band response is shifted on the display when the IF is changed. For maximum accuracy, the HP 8559A front panel adjustment procedure should be repeated when switching to or from ALT IT (see Chapter 1).

IMPROVING AMPLITUDE MEASUREMENT ACCURACY – IF SUBSTITUTION

A technique called IF substitution can be used to improve the accuracy of spectrum analyzer amplitude measurements. IF substitution involves using only the accurate IF gain of the spectrum analyzer to position an unknown signal at the calibrated REFERENCE LEVEL line. Errors caused by the log amplifier, input attenuator, bandwidth filters, and CRT are eliminated because they are left unchanged throughout the measurement. The IF gain of the spectrum analyzer is controlled with the calibrated REFERENCE LEVEL control.

Amplitude Measurement with IF Substitution

The steps for achieving accurate amplitude measurements with IF substitution are as follows:

1. Set the INPUT ATTEN control to 10 dB or greater. This ensures a good input SWR to minimize mismatch errors.

2. Set the FREQUENCY SPAN/DIV and RESOLUTION BW controls to the settings desired for the measurement.

3. If an absolute-amplitude measurement is to be made, connect a calibrated reference signal (CAL OUTPUT, for example) to the spectrum analyzer and verify absolute-amplitude calibration.

4. If a relative-amplitude measurement is to be made, connect the reference signal (unmodulated carrier signal, etc.) to the spectrum analyzer and use the TUNING control and FREQUENCY BAND push buttons to properly tune the signal to the CRT center. Use the REFERENCE LEVEL control and FINE vernier to position the signal peak at the CRT top graticule line, and note the control reading.

5. Connect the signal to be measured and use the TUNING control and FREQUENCY BAND push buttons to properly tune the signal to the CRT center. Use only the REFERENCE LEVEL control and FINE vernier to position the signal peak at the CRT top graticule line.

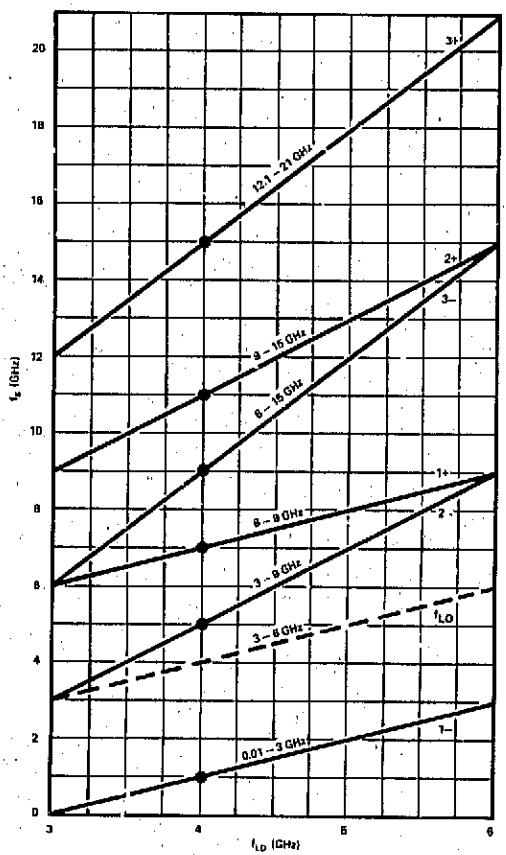


Figure 18. Image Responses

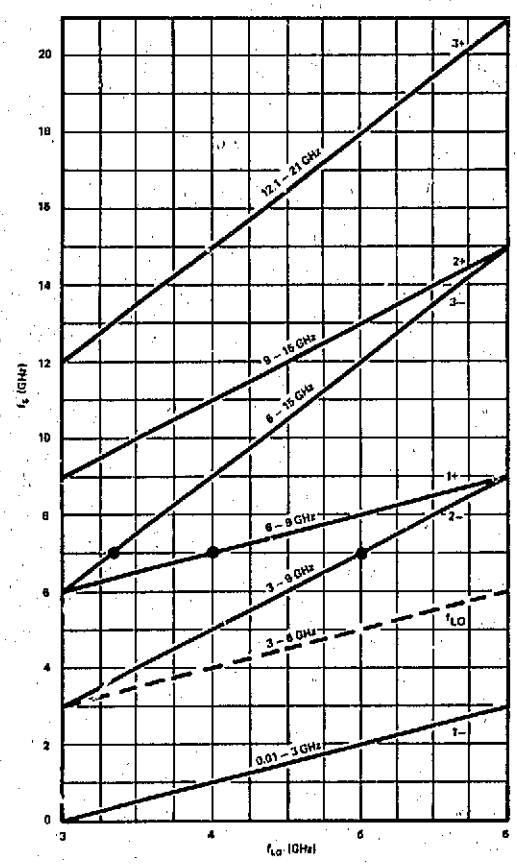


Figure 19. Multiple Responses

6. Note the REFERENCE LEVEL control reading. For relative-amplitude measurements, subtract this reading from the reading in step 4 to determine the amplitude difference in dB.

When the IF-substitution technique is used for amplitude measurements, the only remaining measurement uncertainties are due to the calibrated reference signal, frequency response flatness, and REFERENCE LEVEL control accuracy of the spectrum analyzer. Uncertainties due to log amplifier fidelity, CRT nonlinearities, RESOLUTION BW switching and INPUT ATTEN error are eliminated.

Further improvement in accuracy can be achieved by calibrating the spectrum analyzer at the same frequency at which the measurement will be made. Since this eliminates any flatness uncertainties, measurement accuracy depends only upon the accuracy of the calibration signal and the REFERENCE LEVEL control.

CHAPTER 4
TYPICAL MEASUREMENTS

DISTORTION

Distortion measurement is an area in which the spectrum analyzer makes a significant contribution. Two basic types of distortion are of particular interest: harmonic distortion and two-tone, third-order intermodulation distortion. The HP 8559A, 8558B, and 8557A can measure harmonic distortion products and third-order intermodulation products more than 70 dB down, depending on signal separation and frequency. Refer to the discussion on Maximum Dynamic Range in Chapter 3.

Amplifiers

All amplifiers generate some distortion at the output, and these distortion products can be significant if the amplifier is overdriven with a high-level input signal. The test setup in Figure 20 was used to measure the third-order intermodulation products of a microwave field-effect transistor (FET) amplifier. Directional couplers and attenuators were used to provide isolation between sources.

Figure 21 is a CRT plot for a two-tone, third-order intermodulation measurement. The close-in third-order products ($2f_1 - f_2$ and $2f_2 - f_1$) are visible as low-level signals on each side of the two-tone signals (f_1 and f_2).

Mixers

Mixers use the non-linear characteristics of an active or passive device to achieve a desired frequency conversion. As a result some distortion at the output is due to the inherent non-linearity of the device. Figure 22 illustrates the test setup and CRT plot of a typical mixer measurement. In the example, the RF and LO input signals for a particular mixer were also measured with the spectrum analyzer, and the following information on mixer performance was calculated:

Conversion loss (SSB):

$$RF_{in} - IF_{(+)} = (-20) - (-34) = 14\ dB$$

LO to IF isolation:

$$LO_{in} - LO_{out(IF)} = (+5) - (-28) = 33\ dB$$

RF to IF isolation:

$$RF_{in} - RF_{out(IF)} = (-20) - (-48) = 28\ dB$$

Third-order distortion product (2 LO – RF):

– 58 dBm at 398 MHz.

Oscillators

Distortion in oscillators may be harmonically or non-harmonically related to the fundamental frequency. Non-harmonic oscillator outputs are usually termed spurious. Both harmonic and spurious outputs of an oscillator can be minimized with proper biasing and filtering techniques. A spectrum analyzer can monitor changes in distortion levels while modifications to the oscillator are made. In the full-band or wide span modes, harmonically related responses can be easily identified. Figure 23 is a CRT plot of the fundamental frequency and second harmonic output of an RF oscillator.

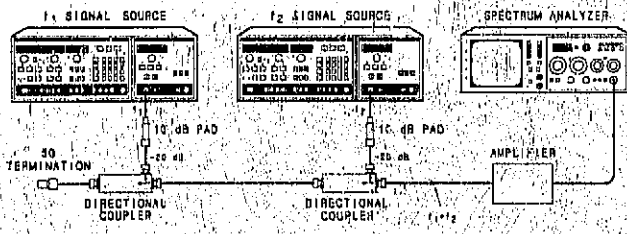


Figure 20. Two-Tone Test Setup

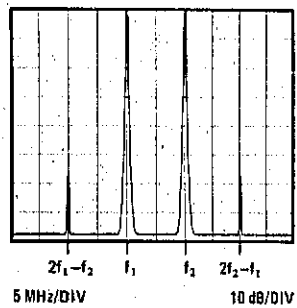


Figure 21. Two-Tone, Third Order Intermodulation Products

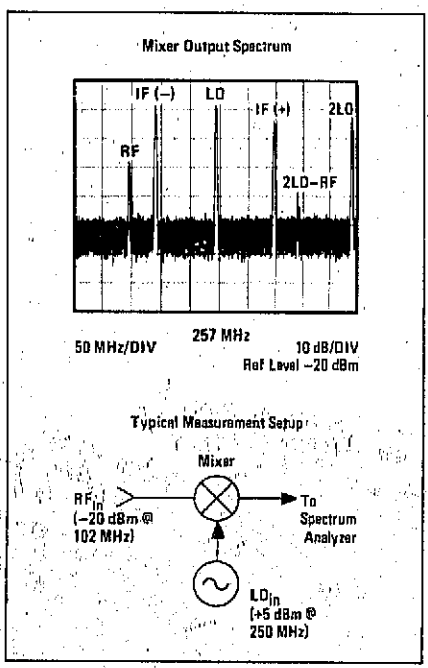


Figure 22. Mixer Measurement

NOTE

Consult HP Application Note AN 150-11 for more information on distortion measurements.

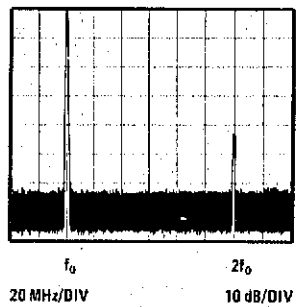


Figure 23. Oscillator Fundmental and Second Harmonic

MODULATION

Amplitude Modulation

The wide dynamic range of the spectrum analyzer allows accurate measurement of modulation levels. For example, the spectrum analyzer can display a 0.06 percent AM signal as a carrier with 70 dBc sidebands. Figure 24 shows a signal with 0.6 percent AM displayed, a log ratio of 50 dB.

Percent AM can be determined from the display with the following equation:

$$\text{Percent AM} = 200 \text{ Log}^{-1}(\text{XdBc}/20)$$
$$= 200 \text{ Log}^{-1}(-50/20)$$
$$= 0.63\%$$

Where X is the dB ratio between the carrier and the sideband

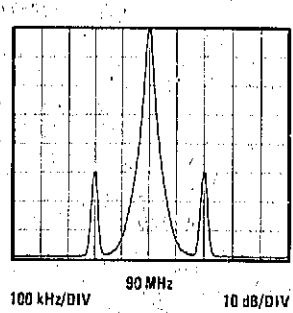


Figure 24. 0.6 Percent AM

When the spectrum analyzer is used as a manually tuned receiver (Zero Span), the AM signal can be demodulated and viewed in the time domain. To demodulate an AM signal, uncouple the RESOLUTION BW and set it to a value at least twice the modulation frequency. Then set the Amplitude Scale to LIN and center the signal, horizontally and vertically, on the CRT. Select ZERO SPAN and VIDEO trigger for a stable trace. The modulation will be displayed in the time domain. (Refer to Figure 25.) The time variation of the modulation signal can then be measured with the calibrated SWEEP TIME/DIV control.

Percent AM can also be determined from the time domain display with the following equation

$$\text{Percent AM} = 100\,(E_{max} - E_{min}/E_{max} + E_{min})$$
$$= 100 \times (7\text{ div.} - 1\text{ div.}/7\text{ div.} + 1\text{ div})$$
$$= 75\%$$

The example shown in Figure 25 demonstrates sinusoidal amplitude modulation, which can be used for narrowband sine wave testing of components and systems. In some cases though, the modulation is not a pure sine wave; however, the spectrum analyzer can still be used to obtain signatures (reference responses) of random modulation for comparison, and as a fixed-tuned receiver which, with headphones connected to its VERTICAL OUTPUT receptacle, can be used to listen to the detected output.

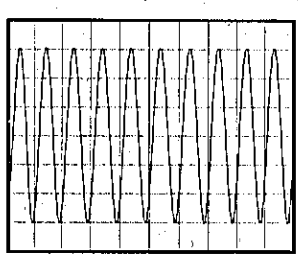


Figure 25. Demodulated AM Signal in Zero Span

Frequency Modulation

For frequency modulated signals, parameters such as modulation frequency (f_m), modulation index (m), and peak frequency deviation of carrier (Δf_{peak}) are all easily measured with the spectrum analyzer. The FM signal in Figure 26 was adjusted for the carrier null which corresponds to m = 2.4 for the *Bessel* function. The modulation frequency f_m is 100 kHz, the frequency separation of the sidebands. The peak frequency deviation of the carrier (Δf_{peak}) can be calculated using the following equation:

$$m = \Delta f_{peak}/f_m$$

or $\Delta f_{peak} = 2.4 \times 100\text{ kHz} = 240\text{ kHz}$

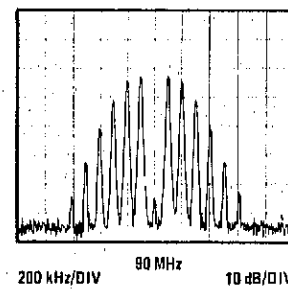


Figure 26. FM Signal Spectrum

If the FM signal displayed does not correspond to a specific carrier or sideband null, the Δf_{peak} can be measured directly, and the modulation index (m) can be calculated.

Although the spectrum analyzers do not have built-in discriminators, FM signals can be demodulated by slope detection. Rather than tuning the signal to the center of the CRT as in AM, the slope of the IF filter is tuned to the center of the CRT. At the slope of the IF filter, the frequency variation is converted to amplitude variation. In FM, the resolution bandwidth must be increased to yield a display similar to that shown in Figure 27 before switching to Zero Span. Note that Δf_{peak} can be determined directly from this display. When Zero Span is selected, the amplitude variation is detected by the spectrum analyzer and displayed in the time domain as shown in Figure 28.

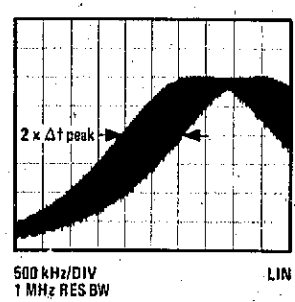


Figure 27. Proper Tuning for Slope Detection (in Hz/Div Mode with Wide Resolution Bandwidth)

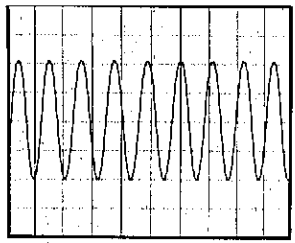


Figure 28. Demodulated FM Signal in Zero Span

NOTE

Refer to HP Application Note AN 150-1 for further information on AM and FM measurements.

Pulsed RF

A pulsed RF signal is basically an RF signal which is turned on periodically for brief intervals of time. Some parameters to be determined in measuring pulsed RF signals are pulse repetition frequency (PRF), pulse width, duty cycle, on-off ratio of the modulator, and pulse power. Pulse power can refer to either the average power or to the peak power of the pulse.

The spectrum analyzer can display a pulsed RF signal in either of two modes, the line mode or the pulse mode. The factor that determines the display mode is the number of spectral components or lines that are in the passband of the spectrum analyzer at any one time. In the line mode, there is only one spectral component or line in the passband; i.e., the spectrum analyzer resolution bandwidth is less than the PRF. In the pulse mode, there is more than one spectral line in the passband; i.e., the spectrum analyzer resolution bandwidth is greater than about twice the PRF.

Since a spectrum analyzer does not display the actual peak pulse power of the signal (a pulsed signal has its power distributed over a number of spectral components, each component representing a fraction of the peak pulse power), a correction of desensitization factor must be added to the displayed main lobe power of the pulsed RF signal to obtain the peak pulse power. The calculation of the desensitization factor depends on whether the spectrum analyzer is displaying the signal in the line or pulse mode.

Line Mode

To obtain a *line* spectrum on the spectrum analyzer, the rule of thumb to follow is that the resolution bandwidth must be less than the PRF. This ensures that individual spectral lines will be resolved. From the line spectrum shown in Figure 29, it is possible to measure the following parameters:

PRF = 50 kHz (spacing between spectral lines)

Main lobe width = 800 kHz

Main lobe power = −41 dBm

Then, based on the above measurement, the following data can be calculated:

Pulse width = 2/Main Lobe width

= 2/800 kHz = 2.5 μsec

Duty cycle = 2 PRF/Main Lobe width

= 2(50 kHz)/800 kHz = 0.125

To determine the peak pulse power for a line spectrum, a pulse desensitization factor (α_L) must be added to the measured main lobe power. The desensitization factor is a function of the duty cycle and is represented by the following equation:

$$\alpha_L = 20 \log (\text{duty cycle})$$

For a 0.125 duty cycle, $\alpha_L = -18$ dB. Hence the peak pulse power in Figure 29 is −23 dBm.

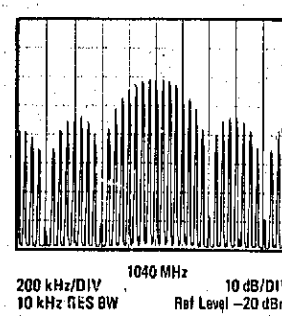


Figure 29. Pulsed-RF Line Spectrum

Pulse Mode

To obtain a pulse spectrum on the spectrum analyzer, the resolution bandwidth must be set to greater than about twice the PRF, to ensure that more than one spectral line is within the analyzer passband. To find the peak pulse power in the pulse mode, add the pulse desensitization α_p, which is a function of pulse width and spectrum analyzer impulse bandwidth, to the main lobe power.

$$\alpha_p = 20 \log (\text{pulse width} \times \text{Impulse BW})$$

Figure 30 illustrates a signal in the pulse spectrum mode. As with the line spectrum, the pulse width can be determined from the main lobe width, while the impulse bandwidth is a characteristic of the analyzer. The impulse bandwidth is approximately 1.5 times the 3 dB bandwidth.

For a pulse width of 2.5 μsec and an impulse bandwidth of 150 kHz, $\alpha_p = -8$ dB. The peak pulse power of the signal shown in Figure 30 then, is -23 dBm.

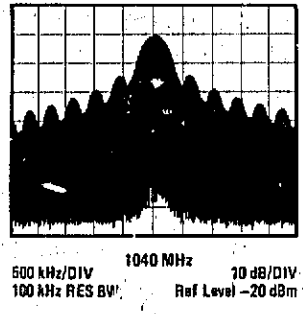


Figure 30. Pulse-RF Pulse Spectrum

Using the pulse spectrum enables a wider resolution bandwidth to be used. The wider resolution bandwidth provides two advantages: First, the signal-to-noise ratio is increased because the pulse amplitude increases linearly with the resolution bandwidth while random noise increases proportionally to the square root of the resolution bandwidth. The only limitation is that the bandwidth should be no greater than about 5 percent of the main lobe width. Secondly, faster sweep times can be used because of the wider resolution bandwidths. The HP 8559A, 8558B, and 8557A all have a 3 MHz resolution bandwidth which enables them to effectively display pulsed RF signals in the pulse mode. The 3 MHz bandwidth, along with fast sweep times, also enables narrow pulse widths to be measured in the time domain. A demodulated pulsed RF signal is shown in Figure 31.

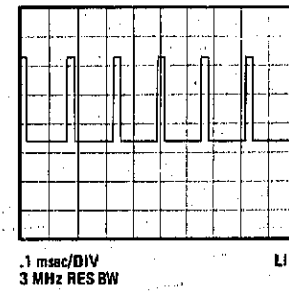


Figure 31. Demodulated Pulsed RF Signal in Zero Span

Few operating pulsed RF systems have ideal spectra. Measurements can still be made regardless of the asymmetry of the spectrum. Examples of non-ideal spectra are found in digital communications and radar.

Since most radar systems do not have ideal spectra, the spectrum of a properly operating system is often stored away for future reference. This reference or spectral signature can then be used to determine changes that would indicate potential problems. An HP 853A based system has the capability of storing display information onto magnetic tape via HP-IB or directly plotting the information (hard copy) for use later (refer to Chapter 2).

In digital communications, the limits placed on transmissions by regulatory agencies are a major concern. If the HP 853A is used with a controller, specification limits can be written directly onto the CRT, thereby making conformance testing less tedious.

Additional factors to consider when measuring pulsed RF signals are the spectrum analyzer VIDEO FILTER control and the digital averaging capability of the HP 853A Display. In general, the VIDEO FILTER and DGTL AVG should be OFF when measuring pulsed RF signals. Adding video filtering or digital averaging will desensitize a pulsed signal and limit its displayed amplitude.

NOTE

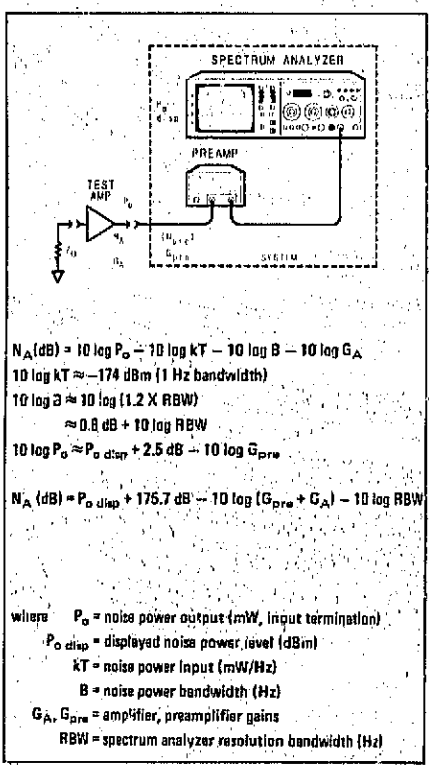
Consult HP Application Note AN 150-2 for more information on pulsed RF measurements.

NOISE

Typical spectrum analyzer noise measurements include oscillator noise (spectral purity), signal-to-noise ratio, and noise figure. The MAX position of the VIDEO

FILTER control and the digital averaging capability of the HP 853A Spectrum Analyzer Display can be used to measure the spectrum analyzer sensitivity or noise power.

The test setup in Figure 32 can be used to make a swept noise figure measurement of an amplifier. First, the total gain of the preamplifier and amplifier under test is determined. Then, the input of the amplifier is terminated and its noise power is measured. The noise figure of the amplifier is the theoretical noise power (KTB) minus the total gain and the amplifier noise power. An added correction factor of 1.7 dB results in the true noise figure (N_A) of the test amplifier. The correction factor is the sum of the bandwidth, log amplifier, and peak detector corrections required to compensate for errors introduced by these elements in the displayed noise power. Figure 33 is a plot of an amplifier's noise power output.



$N_A(dB) = 10 \log P_o - 10 \log kT - 10 \log B - 10 \log G_A$

$10 \log kT \approx -174$ dBm (1 Hz bandwidth)

$10 \log B \approx 10 \log (1.2 \times RBW)$

≈ 0.8 dB + 10 log RBW

$10 \log P_o \approx P_{o\,disp} + 2.5$ dB $- 10 \log G_{pre}$

$N_A(dB) = P_{o\,disp} + 175.7$ dB $- 10 \log (G_{pre} + G_A) - 10 \log RBW$

where P_o = noise power output (mW, input termination)

$P_{o\,disp}$ = displayed noise power level (dBm)

kT = noise power input (mW/Hz)

B = noise power bandwidth (Hz)

G_A, G_{pre} = amplifier, preamplifier gains

RBW = spectrum analyzer resolution bandwidth (Hz)

Figure 32. Measuring Noise Figure — Absolute Power Technique

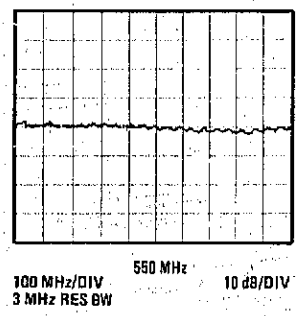
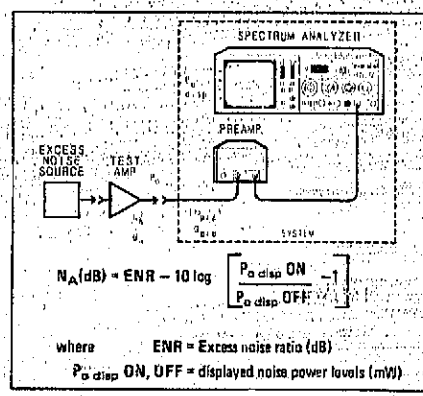


Figure 33. Noise Power Measurement

Another technique, called the Y-Factor Technique (refer to Figure 34), overcomes the problems associated with the analyzer's absolute accuracy by using a calibrated noise power standard, such as the HP 346B Excess Noise Source. By measuring the ratio of P_o with the noise source ON, to P_o with noise source OFF (the test amplifier input terminated in Z_o impedance) we can determine noise figure to a much greater accuracy. Spectrum analyzer *instrument* errors in the relative measurement of P_o ON/P_o OFF are typically less than a few tenths of a dB, leading to measurement accuracies approaching those of a noise figure meter. Figure 35 shows the results of a Y-Factor measurement.

NOTE

Consult HP Application Notes AN 150-4, AN 150-7 and AN 150-9 for more information on noise measurements.



$$N_A(dB) = ENR - 10 \log \left[\frac{P_{o\,disp}\ ON}{P_{o\,disp}\ OFF} - 1 \right]$$

where ENR = Excess noise ratio (dB)

$P_{o\,disp}$ ON, OFF = displayed noise power levels (mW)

Figure 34. Measuring Noise Figure — Y Factor Technique

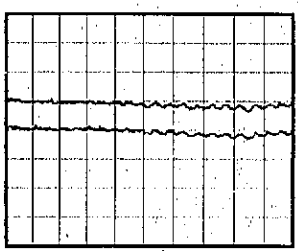


Figure 35. Y-Factor Measurement

ELECTROMAGNETIC INTERFERENCE (EMI)

The objective of EMI measurements is to ensure compatibility between devices operating in the same vicinity. The spectrum analyzer, along with an appropriate transducer, is capable of measuring either conducted or radiated EMI and can also be used as a calibration tool for EMI susceptability testing. Figure 36 illustrates an equipment setup used for measuring radiated field strength.

The antenna in Figure 36 is used to convert the radiated field to a voltage for the spectrum analyzer to measure. The field strength is the spectrum analyzer reading plus the antenna correction factor.

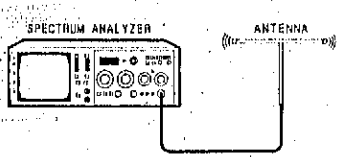


Figure 36. Field Strength Test Setup

Compatability is also important for high-frequency circuits which are in close proximity to each other. In a multi-stage circuit, parasitic oscillation from one stage can couple to a nearby stage and cause unpredictable behavior. A popular technique used to search for spurious radiation uses an inductive loop probe. The loop probe is a few turns of wire that attaches to the spectrum analyzer with a flexible coaxial cable. (Refer to Figure 37.)

Various parts of the circuit can be "probed" to identify the location as well as the frequencies and relative amplitudes of spurious signals. Once the spurious signal has been identified, design techniques can be implemented to reduce or eliminate the cause of interference.

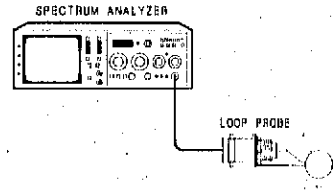


Figure 37. Loop Probe

When testing to detailed EMI specifications (i.e., MIL-STD), it is the worst case limits or the peaks of the signals that are of concern. MAX HOLD on the HP 853A can be used to store the maximum amplitudes of these signals for later comparison with specified limits.

With interface to a desktop computer, an HP 853A-based system can output data automatically and reformat the display to include test limits with the required impulse bandwidth normalizations and antenna factor or current probe corrections.

NOTE

Consult HP Application Notes AN 150-10 and AN 142 for more information on EMI measurements.

SWEPT-FREQUENCY RESPONSE

Frequency response measurements are a common requirement for many system components such as filters, amplifiers, and mixers. The addition of an appropriate source to the spectrum analyzer makes a powerful system for stimulus/response (swept-frequency) measurements.

The HP 8444A Option 059 is a tracking generator with an RF output frequency that follows (tracks) the tuning of the HP 8558B spectrum analyzer over the frequency range of 500 kHz to 1500 MHz. Since the first local oscillator from the spectrum analyzer is used as a reference by the tracking generator, any drift or residual FM is transferred to the tracking generator. The frequency spans of the two instruments are matched and synchronous, providing precise signal tracking. The equipment setup for this measurement is shown in Figure 38.

A significant advantage of the spectrum analyzer/tracking generator combination for swept measurements is the large dynamic range. Noise is bandwidth-limited in the spectrum analyzer, and harmonics and spurious products are not limiting factors since the spectrum analyzer is **always** tuned to the fundamental of the tracking generator. The dynamic range for the tracking generator/spectrum analyzer system extends from the output available on the

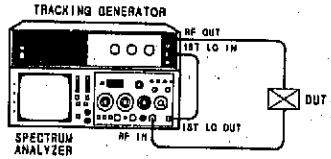


Figure 38. Swept Frequency Test Setup

tracking generator to the noise floor of the spectrum analyzer. For the HP 8558B/8444A Option 059 system, the dynamic range is generally greater than 90 dB. Figure 39 illustrates the large dynamic range that is possible using the HP 8444A Option 059 and the HP 8558B.

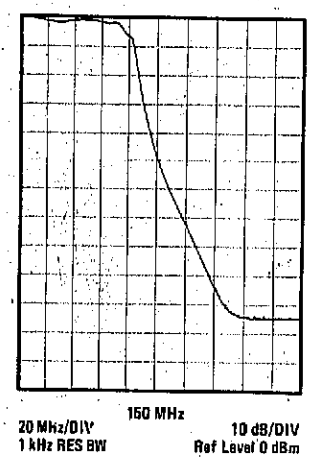


Figure 39. Swept-Frequency Measurement (Composite Plot for Low-Pass Filter with >100 dB of Stop-Band Rejection)

With the HP 853A, the system frequency response can be eliminated from the measurement results by using the **INP – B→A** mode. First, calibrate the system with a known standard (i.e., a through-line for transmission measurements). Then, store the displayed response in Trace B by using either **STORE VIEW** or **STORE BLANK**. Next, insert the device under test and press **INPUT – B→A**. The displayed frequency response is that of the device, not of the system plus the device (refer to Chapter 2 for further details).

NOTE

Errors due to mismatch uncertainty are not removed from measurement by normalization.

The HP 8444A Option 059 can be used with a counter to make accurate, highly sensitive and very selective frequency measurements of unknown signals. Providing a signal can be resolved on the spectrum analyzer, it can be counted. The system can count signals down to the sensitivity of the spectrum analyzer with the frequency accuracy several orders of magnitude better than the spectrum analyzer accuracy.

NOTE

Consult HP Application Notes AN 150-3 and AN 150-13 for more information on Swept-Frequency Response measurements.

CATV MEASUREMENTS

The spectrum analyzer is an important tool for making CATV system measurements. Measurements of signal level, signal frequency, sideband amplitude and frequency, noise, and interference are possible.

Any signal within the passband of a TV channel that causes degradation in the quality of signal reception is called an interference signal. Intermodulation hum and cross-modulation are interference signals which commonly originate within a CATV system. Co-channel interference and radiated interference are also commonly encountered and readily measured with a spectrum analyzer. Co-channel interference occurs when more than one signal competes for the same channel. A co-channel interference signal appears as an unmodulated sideband separated from the main carrier signal by 10 or 20 kHz.

The standard economy spectrum analyzers have an input impedance of 50 ohms; for 75-ohm CATV measurements, an HP 11694A Matching Transformer is recommended. In making amplitude measurements, the performance characteristics of the HP 11694A must be taken into account. Options for the HP 8557A and 8558B are available which allow measurements in 75-ohm systems directly, providing dBm or dBmV calibration.

NOTE

Consult the HP Cable Television Systems Measurements Handbook (HP Part Number 5955-8509) for more information on CATV measurements.

CHAPTER 5
HP-IB REMOTE OPERATION

This chapter provides information about remote operation of the HP 853A Spectrum Analyzer Display (with a compatible spectrum analyzer plug-in) using an HP-IB[1] controller.

General Description

The HP 853A Spectrum Analyzer Display can be accessed for remote operation through HP-IB. The HP-IB connector and address switch are on the instrument rear panel. Interconnection between the HP 853A and the HP-IB controller is accomplished with an appropriate HP-IB interface, and may require an additional HP-IB interconnection cable (often supplied as an integral part of the HP-IB interface).

Communication between instruments on the HP-IB requires that a unique address be assigned to each instrument. The rear-panel address switch (Figure 40) is used to set the HP-IB address of the HP 853A.

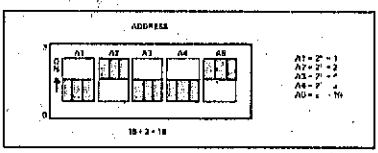


Figure 40. HP-IB Address Switch

HP-IB Capability

The complete bus capability of the HP 853A, as defined in IEEE STD 488 (or identical ANSI Standard MC1.1), is outlined in Table 4. Instrument responses to general bus commands and control signals are described in detail to aid in programming.

Specific HP-IB programming codes for the HP 853A are given in the syntax reference guide at the end of this chapter, and are summarized in Table 5. Sample programs written on an HP 85 controller, in the BASIC programming language, are presented in Appendix B to demonstrate the use of these programming codes.

[1] Hewlett-Packard Interface Bus, the Hewlett-Packard implementation of IEEE STD 488-1978 and ANSI STD, MC 1.1, "Digital Interface for Programmable Instrumentation."

Digital Display Coordinates

Trace data is stored in the trace memory of the HP 853A using the digital display coordinates shown in Figure 41. In references to the display coordinates for programming codes AP/BP, BA/BB, XY, TA/TB, IA/IB, and JA/JB, the coordinates in Figure 41 apply.

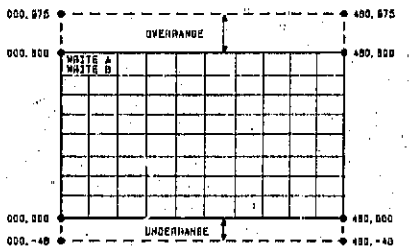


Figure 41. HP 853A Digital Display Coordinates

Within the range of the CRT graticule, there are a total of 481 x-axis values (0 to 480, with 48 points per division) and 801 y-axis values (0 to 800, with 100 points per division). The y-axis overrange values and underrange values are also noted in the figure.

Two lines of annotation near the top of the trace area of the CRT display are controlled by the programming codes CS, LL/LU, LP, and RU/RL.

Syntax Reference Guide

This Syntax Reference Guide is intended to provide, in detail, the required command format to be used when addressing the HP 853A from an external HP-IB controller, and to describe precisely the resulting HP-IB output. It is important to keep in mind that this guide is written from a controller point of view, as user-generated programs will always be executed in the controller, not in the spectrum analyzer display.

A pictorial flow representation is used to delineate the sequence of bytes or blocks of traffic across the bus. Literal ASCII characters are bold and shown in rounded envelopes. These are transmitted exactly as shown. Items

enclosed by rectangular boxes are blocks of bus traffic which require further explanation. Those used repeatedly are:

Output UNL TA21 LA18: UNListen, Talk Address 21, Listen Address 18[2] (ASCII code: ? U2)

Enter UNL LA21 TA18: UNListen, Listen Address 21, Talk Address 18[2] (ASCII code: ?5R)

Additional Commands Additional programming codes (two letter mnemonics) may follow within the same "Output" statement

Note that data bytes passed along the bus originate from the controller (controller is talker) until an "Enter" block is transmitted, at which time the spectrum analyzer display generates any succeeding data (display is talker).

In several cases, two programming codes are used in an identical fashion and are listed together. Each pair performs the same function either on Trace A or Trace B, or on the lower or upper CRT annotation line. Usage of only the first code listed is described; the second code may simply be substituted in its place.

A reference to a "digit" should be understood to refer to the ASCII code for one of the characters 1, 2, 3, 4, 5, 6, 7, 8, 9 or 0.

The HP 853A ignores extra delimiters such as CR (carriage return) and LF (line feed) in a command sequence

[2]Assumes controller address = 21, HP 853A address = 18.

Table 4. HP 853A Responses to General HP-IB Bus Commands

HP-IB Message	Related Mnemonics	Response
Data Trigger	GET	Issues a sweep trigger pulse (for proper use, spectrum analyzer should be in SINGLE SWEEP mode).
Clear	DCL, SDC	Interrupts a sweep in progress. Terminates unfinished commands. Clears any service requests. Resets trace arithmetic reference line to default position (refer to OF command).
		Resets annotation position to top-screen (refer to LP command).
		Resets digital averaging algorithm.
		Resets sweep.
Remote	REN	Enables remote programming of front panel controls.
Local	$\overline{\text{REN}}$, GTL	Front panel controls are not remotely programmable.
Local Lockout	LLO	Locks out local button on front panel (PLOT GRAT/ HP-IB CLEAR).
Require Service	RQS	Instrument may request service (refer to RS command).
Status Byte	SPE, SPD	Serial poll (instrument transmits status byte).
Abort	IFC	Unaddresses instrument.
Response Byte	PPC, PPU	Parallel poll (no response).

The interface functions supported by the HP 853A Spectrum Analyzer Display are: SH1, AH1, T5, L4, SR1, RL1, PP0, DC1, DT1, C0, E2 (as defined in IEEE STD 488-1978 and identical ANSI STD MC1.1).

sent from a controller. However, when the HP 853A is instructed to put out a sequence of data bytes, the complete sequence must be read by the controller before normal operation can be resumed. With the exception of binary trace data transfers (BA and BB), data byte sequences are terminated by transmitting the ASCII characters CR and LF with the End message (EOI bus line pulled "true"). Binary trace data sequences include no terminating CR LF, but the End message is sent during transmission of the final byte of the sequence (the final byte is the 962nd byte for BA and BB).

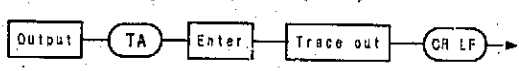
Pressing RESET on HP-IB controllers generates an interface clear (IFC) command on the bus, which unaddresses the HP 853A.

When an illegal two-character mnemonic is received by the HP 853A (one that is not included in the programming code set), bit 5 of the status byte is set and a SYNTAX ERR (error) message is displayed on the upper CRT annotation line. To remove the message, press HP-IB CLEAR (PLOT GRAT) for several seconds, or execute a Clear command over HP-IB.

Table 5. Summary of HP 853A Programming Codes

Mnemonic	Definition	Mnemonic	Definition
TA	Output trace A, decimal (ASCII) values	JA	Input trace A, binary values
TB	Output trace B, decimal (ASCII) values	JB	Input trace B, binary values
BA	Output trace A, binary values		
BB	Output trace B, binary values	CA	Clear (blank) trace A
		CB	Clear (blank) trace B
AP	Output peak coordinates, trace A		
BP	Output peak coordinates, trace B	TS, TSn	Take sweep (n=0–63)
XY	Output coordinates, current point in sweep	RSb	Set Request Service conditions (b=mask)
		OI	Output Device Identification
LU	Input upper CRT annotation line	OFn	Set INPUT–B→A offset (n=0–975)
LL	Input lower CRT annotation line	FP	Output front panel control settings
LPn	Set annotation line position (n=0–8)		
RU	Restore upper CRT annotation line		REMOTE OPERATION (REN enabled)
RL	Restore lower CRT annotation line		
CS	Output character string (CRT annotation lines)	ACn	Set TRACE A control (n=1–4)
		BCn	Set TRACE B control (n=1–4)
		DCn	Set DIGITAL AVERAGE control (n=0–1)
IA	Input trace A, decimal (ASCII) values		
IB	Input trace B, decimal (ASCII) values	ICn	Set INPUT–B→A control (n=0–1)

TA,TB Output trace A, output trace B, decimal (ASCII) values



Trace Out: Sequential y-coordinates (−50 to 975) for trace A or trace B. Format is 481 three-digit coordinates (including leading zeros and minus signs) separated by commas for a total of 1923 ASCII characters. The value −50 indicates a blanked trace.

Example:

	#1	#2	#3	#480	#481
ASCII Sequence	001,	−04,	012, ...	975,	100

BA,BB Output trace A, output trace B, binary values

Trace Out: Sequential y-coordinates (−50 to 975, in two's complement binary form) for trace A or trace B. Format is 481 two-byte coordinates for a total of 962 bytes. The value −50 indicates a blanked trace.

Example:

	#1	#2	#3	.....	#480	#481
Byte sequence	ab	ab	ab	.....	ab	ab

where a and b are 8-bit bytes. To represent the y-coordinate 820, the pair of 8-bit bytes would be

a = 00000011
b = 00110100

AP,BP Output peak coordinates of trace A, trace B

x,y: x,y coordinates (000 to 480, −48 to 975) of single maximum trace peak. Format is two 3-digit coordinates separated by a comma (7 ASCII characters).

Example:

	x	y
ASCII sequence	240,	800

If the peak y-value occurs for two or more values of x, the leftmost point (lowest x-value) is returned.

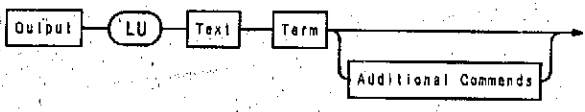
XY Output coordinates, current point in sweep

x,y: x,y coordinates (000 to 480, −48 to 975) of current point in sweep. Format is two 3-digit coordinates separated by a comma (7 ASCII characters).

Example:

	x	y
ASCII sequence	240,	800

LU,LL Input upper, lower CRT annotation line



Text: Up to 60 ASCII characters to appear on upper annotation line (LU) or lower annotation line (LL) on CRT.

Term: An ASCII terminating character ETX, LF, CR, or any byte in the range 0 to 31 decimal.

853A Display Character Set

32*-63	!"#$%&'()*+,-./0123456789:;<=>?
64-95	@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_
96-127	`abcdefghijklmnopqrstuvwxyz{|}~

*Character 32 is a blank

OPERATION

CON'T

LPn Set annotation line position (n = 0 – 8)

n: For n = 1 to 8, positions both lines of CRT annotation in the nth division from the bottom CRT horizontal graticule line.

For n = 0, all CRT annotation is blanked.

Default value is n = 8.

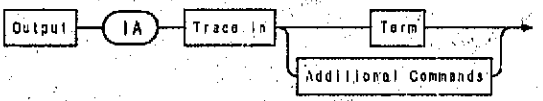
RU,RL Restore upper, lower CRT annotation line

Returns CRT annotation to control labeling mode (clears annotation line sent using LU or LL code).

CS Output character string (CRT annotation lines)

Upper, Lower Line: Two 60-character ASCII strings corresponding to the characters displayed in the upper and lower CRT annotation lines. Each 60-character line is followed by an ETX.

IA,IB Input trace A, trace B, decimal (ASCII) values



Trace In: Sequential y-coordinates (–99 to 975) for trace A or trace B. Values less than –48 are blanked. Format is up to 481 one- to three-digit coordinates (including leading zeros and minus signs), each separated by a comma, space, CR, LF, or combination of these delimiters.

Term: Sequences with less than 481 coordinates must be terminated with a semicolon or additional two-letter programming code. Sequences with 481 coordinates must be terminated by a delimiter (comma, space, CR, LF, or combination) or by an additional two-letter programming code.

Example:

	#1	#2	#3	#4	#5	
ASCII sequence	0,	–4,	800,	–50,	0;	(5 coordinates)

Example:

	#1	#2	#3	#4	#5	
ASCII sequence	0 CR	–4 CR	800 CR	–50 CR	0 TS	(5 coordinates followed by Take Sweep code)

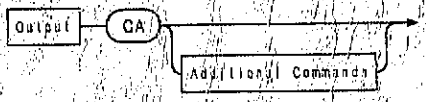
Example:

	#1	#2	#3		#480	#481	
ASCII sequence	–5	100	375	...	100	–5 CR LF	(ASCII spaces between coordinates)

JA,JB Input trace A, trace B, binary values

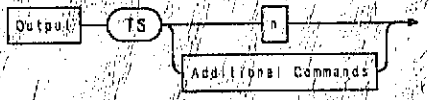
Trace In: Sequential y-coordinates (−99 to 975, in two's complement binary form) for trace A or trace B. Values less than −48 are blanked. Format is 481 two-byte coordinates for a total of 962 bytes. Refer to **BA,BB** codes.

CA,CB Clear (blank) trace A, trace B



Blanks trace (all y-coordinates set to −50).

TS,TSn Take sweep (n = 0 – 63)

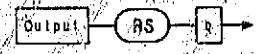


Triggers the spectrum analyzer to sweep and inhibits subsequent commands until sweeping is complete.

n: Specifies number of sweeps to be taken. If n is not specified, one sweep is executed.

During execution of the **TS** and **TSn** commands, the first five bits of the status register define a binary value indicating the total number of full and partial sweeps remaining. The status register may be accessed by a serial poll from the controller, and bit 6 will be low.

RSb Set Request Service conditions (b = mask)



Sets the instrument conditions that will trigger a service request. When one of these conditions occurs, the SRQ line is pulled and two bits of the status register are set – bit 6 and the appropriate bit for the particular service request condition. A serial poll from the controller resets the status register and SRQ line.

b: a one-byte mask for setting service request conditions (SRQ line pulled only by selected conditions). Mask value is set to 0 at power-on.

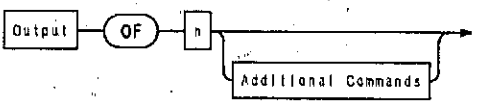
Status Register Bit	Description of Service Condition	Mask Value (Decimal)
0	End of Sweep	1
1	Not used	(2)
2	Fast Sweep Error	4
3	INPUT–B→A Error	8
4	Digital Average/MAX HOLD Error	16
5	Syntax Error	32
6	Universal HP-IB Service Request Bit (set when service condition exists)	(64)
7	Not used	(128)

For example, a mask value of 61 (1 + 4 + 8 + 16 + 32) enables all possible service request conditions. The mask must be sent as the binary byte 00111101.

OI Output Device Identification

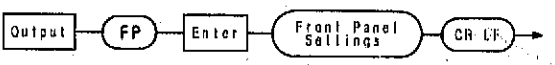
Instrument returns a three-character string, "853", for identification.

OFn Set INPUT – B→A offset (n = 0 – 975)



n: Sets x-coordinate of reference trace during trace arithmetic. Value is initially set to 400 (mid-screen) or 800 (top graticule line) by position of jumper internal to instrument.

FP Output front panel control settings

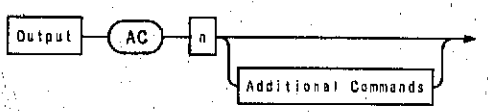


Front Panel Settings: A 12-character string representing current display control settings. Format is twelve ASCII bytes in the form of control setting codes: **"ACmBCmDCnICn"**

where m = 1–4
n = 0,1

REMOTE OPERATION (REN required)

ACn,BCn Set TRACE A, TRACE B control (n = 1 – 4)

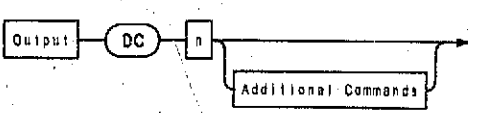


Remotely control trace functions.

n: n = 1 CLEAR WRITE
n = 2 MAX HOLD
n = 3 STORE VIEW
n = 4 STORE BLANK

Remote operation is denoted by a "■" appearing next to display function callouts, just to left of graticule.

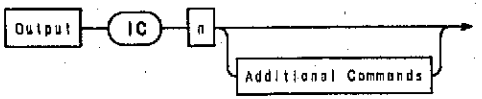
DCn Set Digital Average control (n = 0,1)



Remotely control digital averaging.

n: n = 0 Turn OFF
n = 1 Turn ON

ICn Set INPUT – B→A control (n = 0,1)



Remotely control trace normalization.

n: n = 0 Turn OFF
n = 1 Turn ON

APPENDIX A
AMPLITUDE CONVERSIONS

CONVERSION EQUATIONS

The following equations allow conversion from dBm to dBmV or dBV in a 50Ω system.

dBm + 107 dB = dBμV

dBm + 47 dB = dBmV

dBmV + 60 dB = dBV

If it is desired to convert from logarithmic units to linear units, then the equations given below will be useful. Keep in mind that the logarithmic levels are all referenced to linear units.

That is:

0 dBm referenced to 1 mW
0 dBmV referenced to 1 mV
0 dBμV referenced to 1 μV

To calculate a linear level, simply take the antilog of the logarithmic level.

dBm to P(mW)

$$dBm = 10 \log \frac{P}{1\ mW},\ P = \log^{-1} \frac{dBm}{10}$$

dBmV to V(mV)

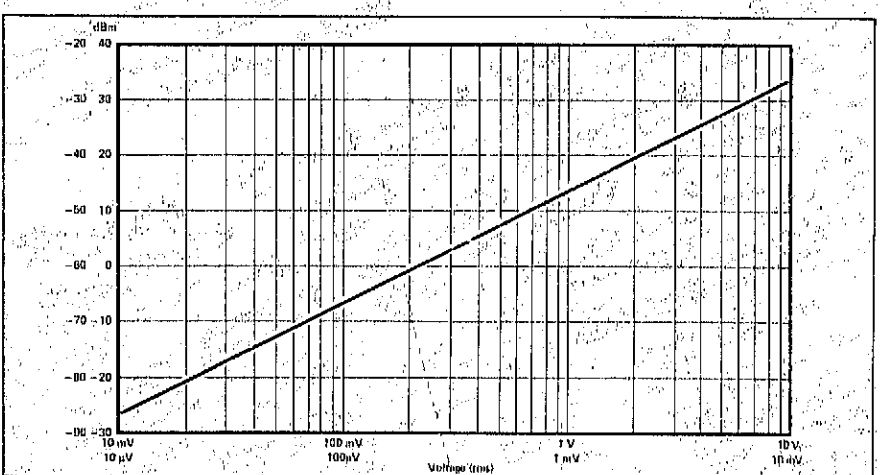
$$dBmV = 20 \log \frac{V}{1\ mV},\ V = \log^{-1} \frac{dBmV}{20}$$

dBμV to V(μV)

$$dB\mu V = 20 \log \frac{V}{1\ \mu V},\ V = \log^{-1} \frac{dB\mu V}{20}$$

Figure A-1 can be used to convert from dBm to voltage in a 50Ω system.

Conversion from dBm to volts can be made whether the Amplitude Scale is in LOG or LIN. To read voltage, position the signal on the reference level line of the CRT. Read the REFERENCE LEVEL in dBm and find its equivalent voltage from the conversion chart.



Conversion Chart, dBm to Voltage (for 50 Ohms)

APPENDIX B
PROGRAMMING EXAMPLES FOR THE HP 853A

The following examples illustrate some of the ways the entire command set of the HP 853A may be used when operated with the HP-85 BASIC language controller. It is assumed that the user has a prior knowledge of controller operation and the BASIC programming language.

The programming codes and examples are divided into four functional categories: Labeling, Trace Data I/O, Sweep Control and Instrument Status, and Display Remote Operation.

A user new to the system should first work through the examples to become familiar with the various programming codes, and then refer back to this Operation manual as needed when developing programs (refer to Chapter 5 for a detailed HP-IB syntax reference guide for the HP 853A).

The following programs assume the selectable interface address is 7 and the HP 853A HP-IB address is set to 18 (see Chapter 5).

If an illegal two-letter mnemonic is sent to the HP 853A (i.e., one that is not included in the programming code set), the message SYNTAX ERR will appear on the CRT. To remove the SYNTAX ERR message, send the command CLEAR or press HP-IB CLEAR (PLOT GRAT) on the HP 853A front panel for several seconds. Clearing the HP 853A status register also removes the message; refer to the **RS** programming code in Chapter 5 for details.

Labeling

LU,LL Input upper, lower CRT annotation line

The **LU** or **LL** programming code allows the transfer of up to 60 characters selected from the ASCII character set (see **LU,LL** codes in Chapter 5) to each of the two CRT display lines. To demonstrate the use of both display lines with the alphanumeric character set, run the following program:

```
10 OUTPUT 718 ;"LUTHE 853A CAN
   ANNOTATE 60 TOTAL SPACES WIT
   HIN EACH DISPLAY BUFFER"
20 OUTPUT 718 ;"LL0123456789 a
   quick brown fox jumped over
   the lazy dog's back"
```

The controller executes an OUTPUT statement to transfer the character string in a free-field format. To prevent unnecessary bus traffic, compact field formatting transfers no leading or trailing spaces:

```
10 OUTPUT 718 USING "K" ; "LU N
   o extra spaces!"
```

RU,RL Restore upper, lower CRT annotation line

To restore the upper and lower lines of annotation to the power-on condition, use the following commands:

```
10 OUTPUT 718 ;"RU"
20 OUTPUT 718 ;"RL"
```

or

```
10 OUTPUT 718 ;"RU RL"
```

LPn Set annotation line position (n = 0 to 8)

This programming code is provided to change the position of the annotation lines relative to the CRT graticule lines (the bottom graticule line is designated n = 1). It helps ensure that labels do not interfere with a displayed signal. An example program demonstrates the use of the LP code:

```
10 OUTPUT 718 ;"LU THIS IS A TE
   ST!"
20 OUTPUT 718 ;"LP3"
30 OUTPUT 718 ;"LP7"
40 OUTPUT 718 ;"RU RL"
```

The labels can be moved from the turn-on position, n = 8, to other vertical levels, but will be blanked when they interfere with the trace.

CS Output character string (upper, lower CRT annotation lines)

All display annotation can be transferred to a 122-character string, dimensioned in the controller and then printed:

```
10 DIM C$[122]
20 OUTPUT 718 ;"CS"
30 ENTER 718 ; C$
40 PRINT C$
```

The array in line 10 is dimensioned to store the character strings from both annotation lines. A "CS" programming code calls for the transfer of display characters into the string array. Statement 40 results in a display of the character string on the controller. The ASCII controller code for specifying end-of-text (ETX) is included in the character string, accounting for the two extra characters dimensioned.

Trace Data I/O

TA,TB Output trace decimal (ASCII) values
BA,BB Output trace binary values

Speed, storage requirements, and programming convenience govern the choice of trace data output techniques, i.e., the optimum use of the commands **TA,TB** and **BA,BB**. Three different methods follow:

Method I (ASCII decimal data transfer into integer array)

Method I provides fast transfer of all 481 trace values from the HP 853A to a numeric array dimensioned in the controller (≈1.75 sec). After reformatting, the trace data can be processed by the controller. The array storage requirement is 3366 bytes (3 x 481 + 1923 = 3366) of controller memory. The following example includes the transfer of trace data to the controller and reformatting into an integer array:

```
10 DIM A$[1923]
20 INTEGER B(480)
30 OUTPUT 718 ;"TA"
40 ENTER 718 ; A$
50 FOR I=0 TO 480
60 J=4*I+1
70 B(I)=VAL(A$[J,J+2])
80 NEXT I
```

String array A$ is assigned a length of 1923 characters; the numeric array B is dimensioned as a 481-value INTEGER array to save storage space (3 bytes/value vs. 8 bytes/value). The TA instruction is sent and the string A$ is transferred in lines 30 – 40. This string now must be converted to a numeric array of 481 values, accomplished in the For..... .NEXT loop set up in lines 50 – 80.

Method II (Direct ASCII decimal transfer and storage)

Method II is convenient for temporary storage of trace values when no data processing is required. The following example shows the use of the **IA** programming code (which inputs ASCII decimal trace values) to return a stored trace to the HP 853A:

```
10 DIM A$[1923]
20 OUTPUT 718 ;"TA"
30 ENTER 718 ; A$
40 PAUSE
50 OUTPUT 718 ;"IA",A$
```

Method II is convenient because it requires less array storage (1923 bytes), but the data is in string form (conversion is necessary before numerical calculations can be made). The trace transfer time is approximately 1.28 seconds for **TA** and approximately 0.70 second for **IA** (refer to **IA,IB** for further details).

Method III (Fast trace transfer for storage)

When the fastest possible transfer of trace values is required, Method III is the best choice. This method transfers trace values in binary form as quickly as possible for later conversion to a numeric array.

```
10 DIM A$[970]
20 IOBUFFER A$
30 OUTPUT 718 ;"BA"
40 TRANSFER 718 TO A$ FHS
```

A$ is dimensioned 8 bytes more than transferred (i.e., 2 bytes/value x 481 + 8 bytes = 970 bytes). The IO BUFFER statement designates A$ to have a working length of 962 when executed. The **BA** programming code is sent in line 30 to call for a transfer of byte values, and line 40 provides for a fast hand-shake (FHS) TRANSFER. The time required to transfer a full trace is approximately 155 msec.

When it is necessary to convert A$ into numeric data, the following code can be used:

```
50 INTEGER B(480)
60 FOR I=0 TO 480
70 J=2*I+1
80 B(I)=256*NUM(A$[J])+NUM(A$[J
   +1])
90 NEXT I
```

Two 8-bit bytes are required to specify the full range, −48 to 975, of the digital CRT display: the first byte carries the two most significant bits, and the second byte carries the eight least significant bits. To combine each pair of bytes from A$ into a single numeric value, it is necessary to convert both string values to numeric values, multiply the first by $2^8 = 256$, and add it to the second. Note that this program works only for positive trace values; for underrange values, test for 2's complement and make the appropriate conversion.

IA,IB Input trace integer values

These commands allow the controller to output up to 481 integer trace values into trace A or trace B. Values in the range −48 to 975 are displayed at corresponding levels on the CRT; values less than −48 are blanked. **IA** and **IB** are useful for re-entering trace data that has been previously stored using the **TA** or **TB** programming codes (see Method II), or for transferring a controller-generated "trace" (such as a test limit line stored in trace B).

Place the HP 853A display in the CLEAR WRITE A and STORE VIEW B modes, then run the following example:

```
10 OUTPUT 718 ;"IB"
20 FOR I=0 TO 60
30 OUTPUT 718 ;300,300,300,300,
   -50,-50,-50,-50
40 NEXT I
```

The programming code **IB** in line 10 instructs the HP 853A to receive a numeric string of values for trace B. Lines 20−40 set up a sequence of display values for transfer (the value −50 blanks the trace). When the data transfer is complete, the result is a dashed limit line viewed in trace B.

JA,JB Input trace binary values

Data transfer over the interface bus can be performed more rapidly by using the **JA** or **JB** programming codes rather than **IA** or **IB**. The following example shows how these programming codes can be used to compare a stored trace with a current trace:

```
10 DIM A$[970]
20 IOBUFFER A$
30 OUTPUT 718 ;"BA"
40 TRANSFER 718 TO A$ FHS
50 DISP LEN(A$)
•
•
•
90 OUTPUT 718 USING "K,B" ; "JA
   "
100 TRANSFER A$ TO 718 FHS
```

Lines 10 - 50 transfer the 481 two-byte binary values from trace A to the string array A$, with a fast handshake, and then display the length of A$.

In Line 90, the USING "K,B" format is sent with the **JA** programming code to output a string of byte values, with no end-of-line sequence (CR or LF), to the HP 853A. Line 100 causes a fast TRANSFER of data from string A$.

AP,BP Output peak coordinates
XY Output coordinates of current point in sweep

It often happens that the only data point required is the peak value of the 481-point CRT trace. To obtain the x- and y-axis coordinates (0 to 480, 0 to 975) of the maximum response, use the **AP** or **BP** programming code for trace A or trace B respectively. If there is more than one response at the peak level (i.e., two identical values in different "X" locations), then the left-most "X" will be returned after you enter the code:

```
10 OUTPUT 718 ;"AP"
20 ENTER 718 ; X,Y
30 DISP X,Y
```

The x,y coordinates of the current point in a manual sweep can be transferred using the **XY** programming code, allowing the controller to monitor display data while in the manual sweep mode.

```
10 OUTPUT 718 ;"XY"
20 ENTER 718 ; X,Y
30 DISP X,Y
```

Sweep Control and Instrument Status

TS,TSn Take n sweeps (n = 0 to 63)

The **TS** programming code allows the triggering of spectrum analyzer sweeps from a controller. This capability can be used to initiate sweeps when the analyzer is in either the single or continuous sweep mode.

NOTE

It is important to have an updated trace before transferring data.

When sent to the HP 853A, the **TS** programming code triggers a sweep and inhibits subsequent commands until that sweep is complete. Upon completion of the sweep, the system resumes normal operation. Consider the following example:

```
10 OUTPUT 718 USING "#,K" ; "TS
   "
20 BEEP
30 OUTPUT 718 ;"LU No display u
   ntil end-of-sweep."
40 PAUSE
50 OUTPUT 718 ;"RU"
60 OUTPUT 718 ;"TS20"
```

After putting the spectrum analyzer plug-in in single sweep mode, set the sweep time to 0.5 sec/DIV and run this program. Receipt of the **TS** code initiates a sweep, at which time a tone is generated by line 20, indicating that the controller is free to proceed, but the HP 853A is not. The message on line 30 will be displayed on the HP 853A CRT only after the end-of-sweep.

If the USING "#,K" were to be omitted in line 10, the controller would attempt to transmit the usual terminating CR and LF after the ASCII characters TS. These cannot be accepted until the spectrum analyzer has completed its sweep, so line 20 (representing all other controller and non-HP 853A bus activity) would effectively be held up until the end-of-sweep occurs. The USING "#,K" format with the **TS** code allows other bus activity during the sweep.

After the program PAUSE, return the SWEEP TIME/DIV to AUTO and then press CONTINUE on the controller. Line 50 restores the upper display line to normal mode. The **"TS20"** programming code, in line 60, triggers a set of 20 sweeps and holds up bus activity until the set of sweeps is complete.

RSb Set request service conditions (b = mask)

A serial poll may be performed to check the contents of the HP 853A status register, which indicates certain conditions in the instrument (refer to the HP-IB syntax reference guide in Chapter 5). Any combination of conditions can be enabled by sending a request service mask over the bus to the HP 853A (conditions not selected will not pull the SRQ line). For example, to enable all available request service conditions, the mask must be the binary equivalent of the decimal sum of each component, or 61 (1 + 4 + 8 + 16 + 32 = 61). Sending a mask replaces any previous mask enabled in the HP 853A. The mask is set to a default value of 0 at power-on.

The following example program demonstrates the use of the **RS** code along with a series of illegal conditions which, until corrected, will generate SRQ messages and set appropriate bits in the HP 853A status register:

```
10 OUTPUT 718 USING "K,B" ; "RS
   ",61
20 OUTPUT 718 ;"YZ"
30 OUTPUT 718 ;"AC2DC1"
40 S=SPOLL(718)
50 DISP S
60 PAUSE
70 OUTPUT 718 ;"AC1DC1"
80 IF S<>0 THEN GOTO 40
90 LOCAL 718
```

In line 10, the mask value is set to 61, thus enabling all request service conditions. The USING "K,B" format outputs the mask value as one 8-bit byte to the HP 853A. With the mask set, the illegal mnemonic **YZ** sent in line 20 causes the SYNTAX ERR(OR) message to appear on the HP 853A CRT until a serial poll is performed (this error condition has a decimal mask value of 32).

The display state selected in line 30 (refer to **ACn, BCn, DCn** commands) causes an additional request service condition (the decimal value 16 represents this Digital Average/MAX HOLD error state). Note the HP 853A CRT annotation indicating remote control (henceforth called "remote indicators").

In lines 40–50 a serial poll is performed; the decimal value of the status register contents (including the universal HP-IB SRQ bit; a decimal value of 64) is then displayed by the controller. Initially, a value of 112 is returned (16 + 32 + 64 = 112). This serial poll clears the syntax error condition and removes the error message SYNTAX ERR from the HP 853A CRT.

The program stops at the PAUSE statement in line 60. Line 70 is executed by pressing the HP-85 CONTINUE key; this selects a legal display state, removing all service request conditions. The program initiates another serial poll and the value 80 (16 + 64 = 80) is returned, since this was the last status register content prior to clearing all error conditions.

A final press of the CONTINUE key executes one additional serial poll, returning the value 0 to indicate that no enabled service request conditions occurred since the previous serial poll. The instrument is then returned to local control.

OI Output Device Identification

The programming code **OI** can be used to identify whether an HP 853A is connected to the interface bus. The controller identifies a device as an HP 853A if the string "853" is returned when using the following program:

```
10 DIM A$[4]
20 OUTPUT 718 ;"OI"
30 ENTER 718 ; A$
40 DISP A$
```

Display Remote Operation

All HP 853A display states and signal processing modes are programmable over the HP-IB. The HP 853A responds to a remote front panel command the same way it does to a manual front panel change.

ACn,BCn Set trace control

The front panel display state of trace A or trace B can be selected by sending the respective **ACn** or **BCn** programming codes.

The value n takes on the following meanings:

n = 1 for CLEAR WRITE
n = 2 for MAX HOLD
n = 3 to STORE VIEW
n = 4 to STORE BLANK

For example, the following lines can be used to remotely program a new front panel setting:

```
10 OUTPUT 718 ;"AC1"
20 OUTPUT 718 ;"BC2"
```

or

```
10 OUTPUT 718 ;"AC1BC2"
```

Note that a square remote indicator is displayed on the CRT.

DCn Set digital average control
ICn Set INPUT — B→A control
OFn Set INPUT — B→A offset

Display processing of trace data can be controlled remotely using the above programming codes. The value n takes on the following meanings:

DCn: Digital average mode,
n = 0 for Normal
= 1 for Digital average

ICn: Normalize state,
n = 0 for INPUT — B→A OFF
= 1 for INPUT — B→A ON

OFn: Normalize offset state,
n = 0 to 975 for vertical offset value on CRT
(For default values refer to the HP-IB syntax guide)

To achieve digital averaging over, for example, 30 sweeps, place the spectrum analyzer in SINGLE SWEEP mode and RUN this example:

```
10 OUTPUT 718 ;"AC1BC1DC1"
20 OUTPUT 718 ;"TS 30"
30 LOCAL 718
```

FP Output front panel control settings

This command interrogates the HP 853A display for its current front panel control settings. The HP 853A can output the present status of **ACn, BCn, DCn, ICn** over the bus into a 12-character string dimensioned in the controller. This string array can later be passed back to the HP 853A to return the front panel to its original state:

```
10 DIM A$[12]
20 OUTPUT 718 ;"FP"
30 ENTER 718 ; A$
40 DISP A$
 .
 .
 .
80 OUTPUT 718 ;A$
```

CA,CB Clear trace memory

Either trace memory can be completely blanked by sending a **CA** or **CB** programming code to the HP 853A (all values of trace memory are set to −50, indicating blanks).

APPENDIX C
180-SERIES DISPLAYS

The HP 8559A, 8558B, and 8557A Spectrum Analyzer plug-ins are compatible with all HP 180-Series display mainframes. However, the HP 180T-series display mainframes (the HP 180TR, 181T, 181TR, and 182T) are particularly recommended for use with the economy spectrum analyzer plug-ins since they feature medium-persistence CRT phosphor and nonbuffered rear panel auxiliary outputs, compatible with most Hewlett-Packard X-Y Recorders.

HP 182T Display

The HP 182T Display is a cabinet-style mainframe with an extra-large CRT viewing area.

HP 181T Display

The HP 181T Display is a cabinet-style mainframe with a variable persistence/storage CRT. The analog storage feature allows signal traces to be preserved for later viewing or photography. The variable persistence feature is convenient for viewing slower sweeps during narrow-band, wide-span signal analysis.

HP 181TR Display

The HP 181TR Display features the same variable persistence/storage CRT as the HP 181T, but is designed to mount in a standard 19-inch rack or stack with other instrumentation.

HP 180TR Display

The HP 180TR Display mainframe is designed to mount in a standard 19-inch rack or stack with other instrumentation.

180T-Series Display Front Panel Features

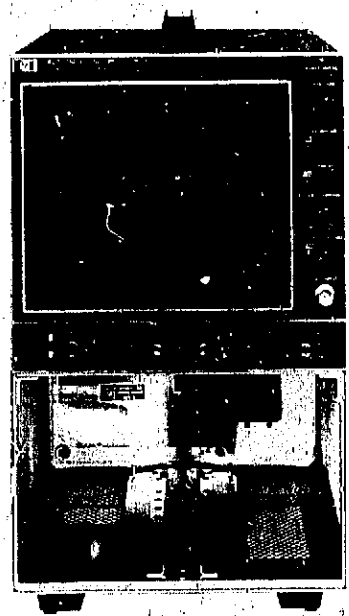
- CALIBRATOR (180TR, 182T): Provides 1 kHz square wave at two amplitudes: 250 mV and 10V p-p (not used with spectrum analyzer).
- Ground Connection (180TR, 182T): Provides chassis ground connection point.
- SCALE (180TR, 182T): Adjusts CRT graticule illumination.
- TRACE ALIGN: Adjusts CRT trace alignment with horizontal graticule lines.
- FOCUS: Adjusts CRT trace sharpness.
- ASTIG: Adjusts CRT spot shape.
- INTENSITY: Adjusts CRT trace intensity.
- FIND BEAM: Intensifies trace and forces on-screen display (normally not used with spectrum analyzer).
- HORIZONTAL POSITION: Single knob provides coarse and fine horizontal adjustment of CRT trace.
- MAGNIFIER: Selects horizontal deflection factor (normally left in X1 position.
- DISPLAY: Selects CRT sweep source (normally left in INT position).
- EXT VERNIER: Provides continuous deflection factor adjustment for external CRT sweep signals. In CAL detent position, deflection factor is selected by MAGNIFIER control (normally not used with spectrum analyzer).
- EXT COUPLING: Selects EXT INPUT ac or dc coupling (normally not used with spectrum analyzer).
- EXT INPUT: BNC input for external CRT sweep signal (normally not used with spectrum analyzer).

NOTE

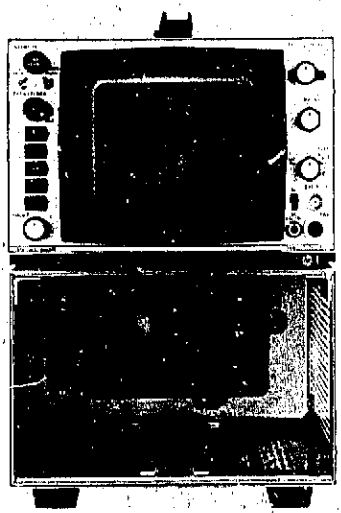
HORIZONTAL EXT INPUT does not sweep the spectrum analyzer first LO. Analyzer should be set to 0 (zero) FREQ SPAN/DIV, AUTO TIME/DIV, and SINGLE SWEEP TRIGGER when operated with an external horizontal input.

180T-Series Display Rear Panel Features

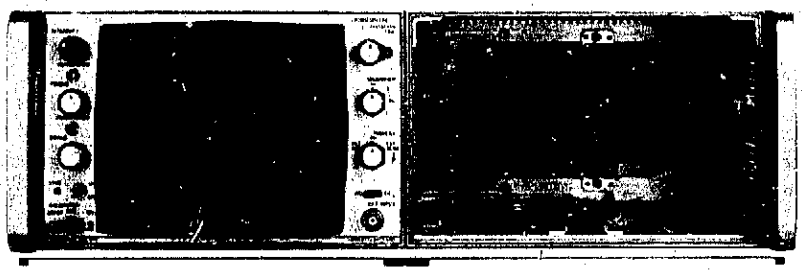
- AUX A Vertical Output: BNC output provides detected video signal from a 50-ohm output impe-



HP 182T DISPLAY



HP 181T DISPLAY



HP 180TR DISPLAY

180-Series Displays

dance. Typical 0–800 mV range corresponds to full 8-division display deflection.

- AUX B PENLIFT/BLANKING OUTPUT: BNC output provides a +15V penlift/blanking signal from a 10K-ohm output impedance when CRT trace is blanked. Otherwise output is low at 0V (low impedance, 150 mA max.) for an unblanked trace.

- AUX C 21.4 MHz IF OUTPUT: BNC output provides 21.4 MHz IF signal (linearly related to spectrum analyzer RF input) from a 50-ohm output impedance. Output bandwidth controlled by spectrum analyzer RESOLUTION BW setting; output amplitude controlled by INPUT ATTEN, REFERENCE LEVEL FINE, and first six REFERENCE LEVEL positions.

- AUX D Horizontal Output: BNC output provides horizontal sweep voltage from a 5K-ohm output impedance. The −5V to +5V range corresponds to full 10-division display deflection.

- Z-Axis Input: BNC input with a 5K-ohm impedance allows external modulation of CRT trace intensity. Approximately +2V blanks normal-intensity trace; negative voltage increases trace intensity. Maximum input voltage ±20 Vdc.

- NORMALIZER INTER-CONN (180TR/182T): Provides connections for HP 8750A Storage Normalizer.

APPENDIX D
CONTROL FUNCTIONS

This appendix identifies and briefly describes the controls used to operate the economy spectrum analyzers and the HP 853A Spectrum Analyzer Display mainframe. For detailed information on the functional capabilities and limitations of individual controls in particular measurement operations, refer to the appropriate paragraphs in Chapters 1 through 4.

FRONT PANEL FEATURES

1. TRACE A, B: Selects CRT display mode for each of two independent digital trace memories.

   CLEAR WRITE: Continuously updates trace memory with current input signal data and displays trace memory contents on CRT.

   MAX HOLD: Updates trace memory with maximum input signal data and displays trace memory contents on CRT.

   STORE VIEW: Current trace memory contents are preserved and displayed on CRT.

   STORE BLANK: Current trace memory contents are preserved without being displayed on CRT.

   ANALOG DISPLAY: CRT display switches to conventional analog display of current input signal when both STORE BLANK push buttons are pressed.

2. DGTL AVG: Activates digital filtering algorithm that averages trace data over successive sweeps. Digital averaging should be restarted after any change in spectrum analyzer control settings.

3. INPUT—B→A: Subtracts contents of trace B memory point-by-point from current input signal data and stores result (normalized input signal data) in trace A memory. Reference line is factory-preset at center horizontal CRT graticule line; normalized trace appears at reference line when input signal data is identical to stored trace B. Reference line indicates 0 dB for relative amplitude measurements.

4. PLOT GRAT/HP-IB CLEAR: Initiates sequence of plotter commands over HP-IB to plot CRT graticule lines (and remotely-programmed annotation). Press push button again to abort active plot. HP-IB plotter must be set to listen-only mode.

   To recover from illegal HP-IB commands (SYNTAX ERR) and to reset display state, press push button for at least 3 seconds to perform HP-IB CLEAR. Instrument returns to LOCAL and discontinues any HP-IB operation in progress.

   Activate digital test routines by pressing PLOT GRAT push button while switching LINE power ON. Push button then selects desired test routine. Press both PLOT GRAT and PLOT TRACE push buttons to revert to normal display state.

5. PLOT TRACE: Initiates sequence of plotter commands over HP-IB to plot displayed CRT trace(s). Press push button again to abort active plot. HP-IB plotter must be set to listen-only mode.

6. LINE: AC line switch. Switches instrument primary power ON and OFF.

7. INTENSITY: Adjusts brightness of CRT trace(s) and annotation characters.

8. SCALE: Adjusts CRT background illumination. SCALE control is disabled in ANALOG DISPLAY mode.

9. Y POSN: Adjusts vertical position of CRT trace. Use Y POSN with reference pattern in digital test routine #4 to align digital trace memory coordinates with corresponding CRT graticule lines.

10. X POSN: Adjusts horizontal position of CRT trace. Use X POSN with reference pattern in digital test routine #4 to align digital trace memory coordinates with corresponding CRT graticule lines.

11. TRACE ALIGN: Rotates trace about center of CRT.

12. FOCUS: Adjusts sharpness of CRT trace.

13. CRT Annotation: Indicates display control settings.

REAR PANEL FEATURES

14. Line Power Receptacle: Three-conductor male receptacle for connecting ac power cable. Power plug retaining bracket, included with standard instrument, can be installed to prevent power cable disconnection when instrument is in transit. Power cable coils on special rear feet when not in use.

15. FUSE: Spring-loaded holder for cartridge-type primary power fuse.

16. SELECTOR (VOLTS): Adapts primary power transformer configuration to voltage of ac primary power source.

17. ADDRESS: Switch settings determine address of instrument to be used for communications via HP-IB. Address is set as sum of the switches, where A5=16, A4=8, A3=4, A2=2, and A1=1.

18. HORIZ (SWEEP) OUTPUT: BNC jack is a sweep output or sweep input, depending on the position of SWEEP switch on Interface Assembly A9. SWEEP switch on assembly A9 is factory set for sweep output (INT).

    As a BNC output, HORIZ (SWEEP) OUTPUT provides horizontal sweep voltage from a 5K-ohm output impedance. The −5V to +5V output range corresponds to a full 10-division CRT horizontal deflection.

    As a BNC input with a 20K-ohm input impedance, HORIZ (SWEEP) OUTPUT allows the CRT display to be swept by a −5V to +5V external horizontal sweep signal (approximately 30V/sec. maximum sweep rate for digital display mode).

19. VERTICAL (VIDEO) OUTPUT: BNC output provides detected video signal from a 50-ohm output impedance. Typical 0–800 mV output range corresponds to full 8-division CRT vertical deflection.

20. BLANK (PENLIFT) OUTPUT: BNC output provides a +15V penlift/blanking signal from a 10K-ohm output impedance when CRT trace is blanked. Otherwise, output is low at 0V (low impedance, 150 mA max.) for an unblanked trace.

21. 21.4 MHz IF OUTPUT: BNC output provides 21.4 MHz IF signal (linearly related to spectrum RF input) from a 50-ohm output impedance. Spectrum analyzer RESOLUTION BW setting controls the output bandwidth. Spectrum analyzer INPUT ATTEN, REFERENCE LEVEL FINE, and the first six REFERENCE LEVEL positions control the output amplitude. Output level is approximately −10 dBm into 50 ohms with a signal displayed at Reference Level.

22. HP-IB Connector: Hewlett-Packard Interface Bus connection allows remote instrument operation and direct digital plotting of CRT display.

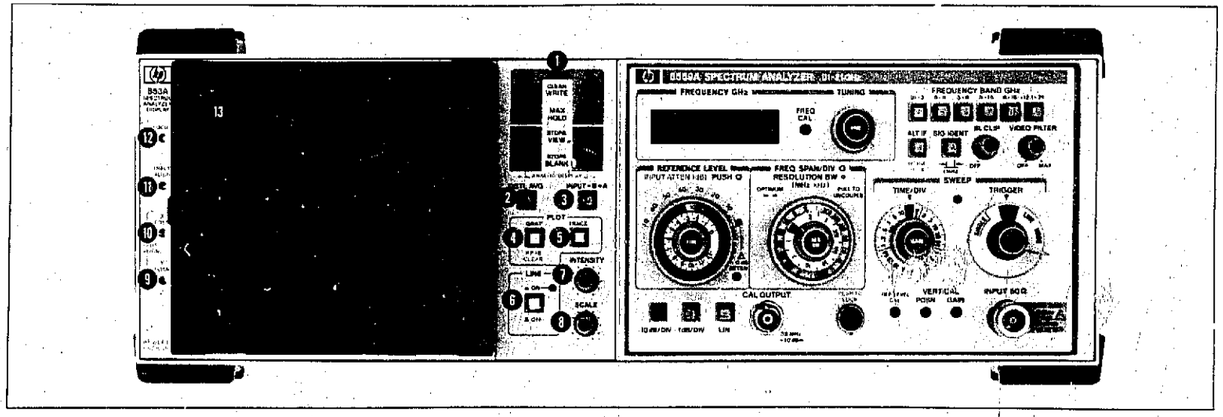


Figure 3-1. HP 853A Front Panel

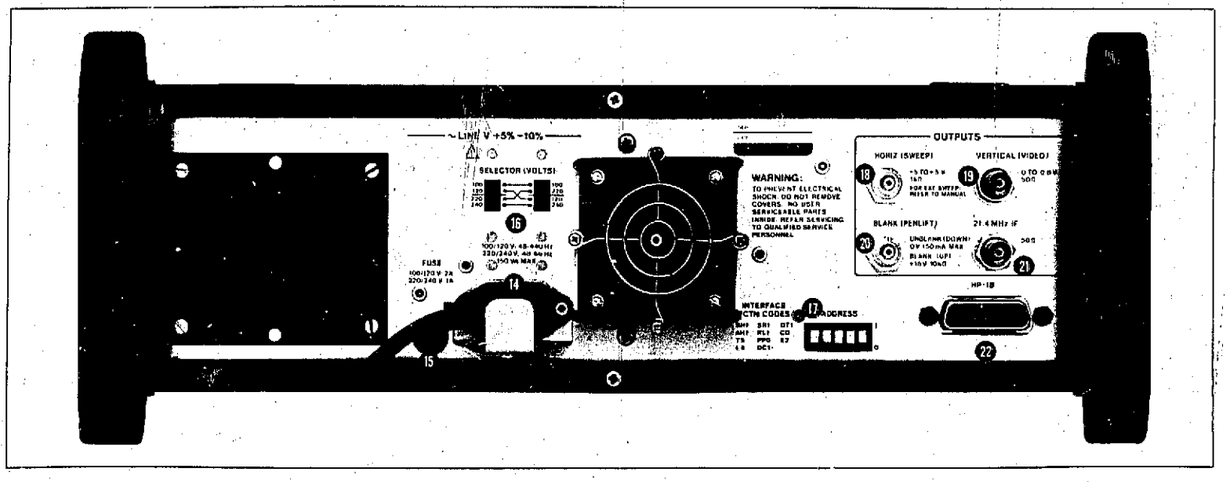


Figure 3-2. HP 853A Rear Panel

ECONOMY SPECTRUM ANALYZER PLUG-INS

FRONT PANEL FEATURES

1. FREQUENCY GHz (HP 8559A): Displays spectrum analyzer center frequency.

2. START–CENTER (HP 8558B, 8557A): Selects mode of FREQUENCY MHz (3) readout.

3. FREQUENCY MHz (HP 8558B, 8557A): Displays spectrum analyzer start or center frequency.

4. FREQ CAL (HP 8559A): Adjusts FREQUENCY GHz (1) readout for calibration on 35 MHz CAL OUTPUT signal.

5. TUNING: Adjusts spectrum analyzer start or center frequency. Coarse tuning is provided by large knob; smaller knob provides FINE tuning.

6. FREQUENCY BAND GHz (HP 8559A): Selects calibrated frequency band. Shifts FREQUENCY GHz (1) readout and adjusts CRT frequency and amplitude calibration for proper display of in-band signals.

7. ALT IF (HP 8559A): Shifts first IF 15 MHz to eliminate baseline lift caused by input signals at approximately 3.0075 GHz.

8. SIG IDENT (HP 8559A): Identifies correct FREQUENCY BAND GHz (6) for unknown signal. Shifts IF and lowers displayed signals on alternate spectrum analyzer sweeps. Correct response is 1 MHz shift to left.

9. VERTICAL POSN: Adjusts vertical position of CRT trace.

10. VERTICAL GAIN: Adjusts deflection circuit gain for amplitude scale calibration of CRT display.

11. FREQUENCY CAL (HP 8558B): Removes tuning hysteresis from first LO (YIG oscillator). FREQUENCY CAL should be pressed before calibration and whenever TUNING (5) is changed by more than 50 MHz.

12. FREQUENCY ZERO (HP 8558B, 8557A): Adjusts FREQUENCY MHz (3) readout for calibration on LO feedthrough (0 Hz).

13. BASELINE CLIPPER: Prevents CRT blooming in variable persistence, storage display mainframes (such as the HP 181T/TR) by blanking the lower portion of the CRT display. When it is operating in its digital display mode, the HP 853A Spectrum Analyzer Display does not respond to this control.

14. VIDEO FILTER: Post-detection low-pass filter smooths CRT trace by averaging random noise. The MAX (detent) position selects 1.5 Hz bandwidth for maximum noise averaging and noise level measurements. The VIDEO FILTER bandwidth is scaled by resolution bandwidth (23) setting. The MAX VIDEO FILTER should not be used for CW signal analysis.

15. SWEEP Indicator: Remains lit during each sweep.

16. SWEEP TRIGGER: Selects sweep trigger mode.

    VIDEO: Sweep triggered on internal post-detection video waveform. One-half major division of vertical deflection (noise, AM signal, etc.) is required to trigger sweep. VIDEO is normally used with 0 (zero) frequency span for time-domain analysis.

    LINE: Sweep triggered at ac line frequency.

    FREE RUN: End of each sweep triggers new sweep.

    SINGLE: Single sweep triggered or reset by turning SWEEP TRIGGER clockwise momentarily.

17. 1st LO OUTPUT (HP 8558B): 50-ohm BNC output provides 2.05–3.55 GHz first LO signal at approximately +10 dBm. Terminate 1st LO OUTPUT with 50-ohm load when not in use.

18. INPUT 50Ω: Precision type N (female) or BNC (female) signal input connector with 50-ohm input impedance.
    Options 001 and 002: INPUT 75Ω–75-ohm BNC (female) signal input connector.

CAUTION

50-ohm BNC connectors might cause damage if used directly with Option 001 and 002 75-ohm BNC INPUT and CAL OUTPUT connectors.

19. SWEEP TIME/DIV: Selects time required to sweep one major horizontal division on CRT.

    AUTO: Automatically selects fastest allowable sweep time as a function of FREQ SPAN/DIV (22), RESOLUTION BW (23), and VIDEO FILTER (14) settings to maintain display amplitude calibration. AUTO operation retained with FREQ SPAN/DIV and RESOLUTION BW controls uncoupled.

    TIME/DIV: Selects calibrated sweep time. TIME/DIV is used primarily with 0 (Zero) frequency span for time-domain analysis of modulation waveforms. Display amplitude calibration not guaranteed for other frequency spans.

    MAN: Enables manual frequency scan using MAN SWEEP knob.

20. PROBE POWER (HP 8558B, 8557A): Provides power for high-impedance active probes, such as the HP 1121A. (See Operation and Service Manual for details regarding use with Options 001 and 002.)

21. REF LEVEL CAL: Adjusts spectrum analyzer RF gain to calibrate top CRT graticule line for absolute amplitude measurements.

22. FREQ SPAN/DIV: Selects CRT horizontal axis frequency calibration.

    MHz/DIV
    kHz/DIV: Selects desired frequency span. Alignment of OPTIMUM markings (▷◁) selects optimum resolution bandwidth (23).

    0 (Zero Span): Spectrum analyzer operates as a manually-tuned receiver, at frequency indicated by FREQUENCY GHz or FREQUENCY MHz readout, for time-domain display of signal modulation.

    F (Full Band-HP 8559A): Spectrum analyzer sweeps entire selected frequency band. FREQUENCY GHz (1) readout corresponds to location of tuning marker displayed on CRT.

    F (Full Span-HP 8557A): Spectrum analyzer sweeps entire frequency range. FREQUENCY MHz (3) readout corresponds to location of tuning marker displayed on CRT.

23. RESOLUTION BW: Selects spectrum analyzer 3-dB bandwidth. Alignment of OPTIMUM markings (▷◁) automatically selects optimum resolution bandwidth for any frequency span. When pushed in, RESOLUTION BW couples mechanically with FREQ SPAN/DIV (22).

24. CAL OUTPUT: BNC (female) output provides calibration signal from 50-ohm output impedance. *Options 001 and 002: 75-ohm output impedance.*

CAUTION

50-ohm BNC connectors might cause damage if used directly with Option 001 and 002 75-ohm BNC INPUT and CAL OUTPUT connectors.

25. 10 dB/DIV–1 dB/DIV–LIN (Amplitude Scale): Selects CRT vertical axis amplitude calibration (logarithmic or linear scale). Reference Level remains constant at top CRT graticule line.

26. REFERENCE LEVEL: Adjusts power level (in dBm or dBmV) represented by top CRT graticule line. Large outer knob adjusts REFERENCE LEVEL in calibrated 10-dB steps; FINE vernier provides 12 dB of continuous adjustment.

27. INPUT ATTEN: Selects desired RF input attenuation, indicated by blue numbers (push and turn).

REAR PANEL FEATURES

28. P1 Connector: Connects spectrum analyzer plug-in to display mainframe.

29. HORIZ GAIN: Allows ±1/2 major division of horizontal gain adjustment to calibrate spectrum analyzer plug-in with HP 180-Series display mainframe.

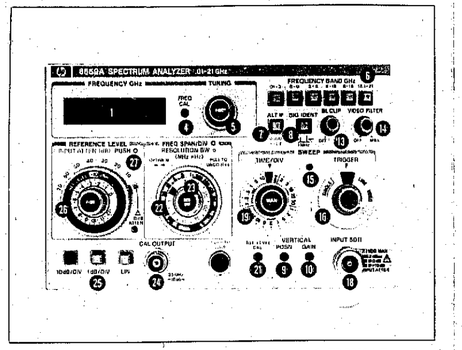


Figure 3-3. HP 8559A Front Panel

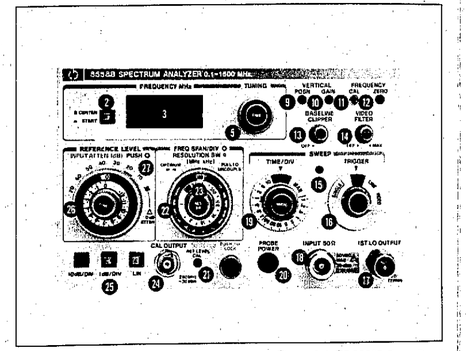


Figure 3-4. HP 8558B Front Panel

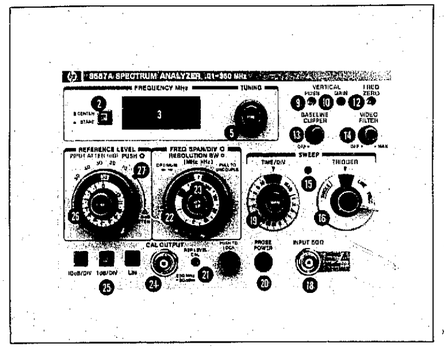


Figure 3-5. HP 8557A Front Panel

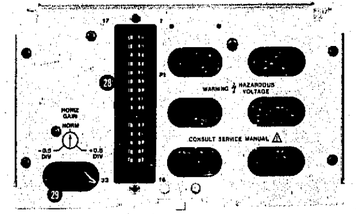


Figure 3-6. Economy Spectrum Analyzer Plug-In Rear Panel

PERFORMANCE CHECK

ADJUSTMENTS

SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The HP Model 853A Spectrum Analyzer Display has no specified performance limits itself; its electrical performance is dependent on the operating parameters of the plug-in spectrum analyzer installed in it. For this reason no performance tests are included in this Operation and Service Manual. All tests required to check the performance of a particular plug-in in combination with the HP 853A Display are provided in the Operation and Service Manual supplied with the plug-in.

4-3. If you merely want to make sure the HP 853A is operating, do the Operation Verification procedure provided in Section II of this manual.

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section describes the adjustments used to restore the HP 853A to its peak operating condition after a repair, or to compensate for changes resulting from component aging. Illustrations showing the appropriate test setups are included in the adjustment procedures. Table 5-1 lists all the adjustments by adjustment name, adjustment reference designator, and by the paragraph number of the adjustment procedure. Included in the table is a brief description of the purpose of the adjustment.

5-3. Data taken during an adjustment should be recorded in the spaces provided in the procedure. Comparison of initial data with data taken during later adjustments is useful for preventative maintenance and troubleshooting.

WARNING

When the covers of the instrument are removed, terminals are exposed that have voltages capable of causing death. The adjustments in this section should, therefore, be performed only by a skilled person who knows the hazard involved.

NOTE

Before performing any adjustments, allow one-half hour warm-up time.

5-4. EQUIPMENT REQUIRED

5-5. Test equipment and accessories required for the adjustment procedures are listed in Table 1-3. If the listed equipment is not available, substitute equipment may be used provided it meets the minimum specifications given in the table.

5-6. Adjustment Tools

5-7. For adjustments that require a non-metallic tuning tool, use fiber tuning tool, HP Part Number 8710-0033 (check digit 4). When a non-metallic tuning tool is not required, you may use an ordinary small, flat-bladed screwdriver or other suitable tool. Regardless of the tool used, do not try to force any adjustment control. Slug-tuning inductors and variable capacitors especially, are easily damaged by excessive force.

5-8. RELATED ADJUSTMENTS

5-9. Related adjustments are those adjustments made with controls that are to some extent interdependent. This interdependency means that when you make a repair in a circuit affected by one of these controls, you must do the adjustment procedures prescribed for all the controls related to the one in the repaired circuit. Related adjustments are listed by their respective groups in Table 5-2.

5-10. FACTORY SELECTED COMPONENTS

5-11. Table 5-3 is a list of factory selected components used in the HP 853A. The components are listed by reference designator, related adjustment paragraph, and by basis of selection. Factory selected components are identified by an asterisk (*) in the schematic diagrams in Section VIII and in the Replaceable Parts lists in Section VI. Part numbers for standard values of selected components are listed in Table 5-4.

Table 5-1. Internal Adjustable Components (1 of 2)

Reference Designator	Adjustment Name	Adjustment Paragraph	Purpose
A3R20	+15V	5-12	Adjusts Display Power Supply +15 volts output.
A3R21	−15V	5-12	Adjusts Display Power Supply −15 volts output.
A3R28	+5.05V	5-12	Adjusts Display Power Supply +5.05 volts output.
A3R30	ASTIG	5-16	Adjusts roundness of spot on CRT.
A3R31	PATTERN	5-16	Corrects for curvature in CRT trace.
A4R4	HV	5-13	Adjusts level of output from High Voltage Power Supply to CRT.
A4R18	INTEN LIM	5-13	Sets maximum CRT trace intensity.
A4R29	FOCUS LIMIT	5-16	Sets range of front-panel FOCUS control.
A5R1	MAX OFF(set)	5-15	Adjusts offset of maximum peak detector output to ADC.
A5R25	MIN OFF(set)	5-15	Adjusts offset of minimum peak detector output to ADC.
A5R50	SWP OFF(set)	5-15	Adjusts offset of horizontal sweep for use by ADC.
A5R52	SWP GAIN	5-15	Adjusts gain of horizontal sweep for use by ADC.
A5R58	ADC OFF(set)	5-15	Adjusts offset of output from Track and Hold amplifier.
A5R71	ADC GAIN	5-15	Adjusts gain of Track and Hold output amplifier.
A5R81	DGTL X GAIN	5-15	Adjusts output level of output from Digital X Generator.
A5R92	DGTL X OFF(set)	5-15	Adjusts output offset voltage of Digital X Generator.
A5R97	STRK GAIN	5-15	Adjusts overall gain of Digital Y Generator.
A5R99	Y FB	5-15	Adjusts magnitude of feedback current in Digital Y Generator.
A5R104	INTEN EQ	5-15	Adjusts relative intensity of short and long CRT strokes.
A6C61	HF TRIM	5-16	Compensates for high-frequency response of Control Gate Amplifier.
A6R2	DGTL Y OFF(set)	5-15	Adjusts digital vertical offset relative to CRT graticule.
A6R4	DGTL Y GAIN	5-15	Adjusts digital vertical gain relative to CRT graticule.
A6R20	X GAIN	5-17	Adjusts gain of X Axis Amplifier.

Table 5-1. Internal Adjustable Components (2 of 2)

Reference Designator	Adjustment Name	Adjustment Paragraph	Purpose
A6R30	Y GAIN	5-17	Adjusts gain of Y Axis Amplifier.
A6R124	INTEN GAIN	5-16	Adjusts the gain of the Voltage-to-Current Converter for a maximum +70V at output of Control Gate Amplifier.
A6R135	DYN FOCUS	5-16	Adjusts amount of intensity dynamic focus correction of CRT display.
A6R151	HF GAIN	5-16	Adjusts high frequency response of Control Gate Amplifier.
A6R153	MIN INTEN	5-13 5-16	Adjusts minimum voltage in Control Gate Amplifier to set minimum CRT trace intensity.
A8R13	+15.05V	5-12	Adjusts +15.05 volts output of Plug-In Power Supply Assembly.
A8R17	−12.65V	5-12	Adjusts −12.65 volts output of Plug-In Power Supply Assembly.

Table 5-2. Related Adjustments

Assembly Replaced or Repaired	Perform the Following Related Adjustments	Paragraph Number
A1 Front Panel Assembly	None	
A1A1 Display Control Assembly	None	
A2 Display Adjust Assembly	Front Panel Adjustments	Sect. III, Chap. 1
A3 Display Power Supply Assembly	Low-Voltage Power Supply Adjustments Digital Storage Adjustments Z Axis Adjustments Analog Deflection Adjustments	5-12 5-15 5-16 5-17
A4 High-Voltage Power Supply Assembly	High-Voltage Power Supply Adjustments Z Axis Adjustment	5-13 5-16
A5 Data Converter Assembly	Digital Storage Adjustments Analog Deflection Adjustments	5-15 5-17
A6 XYZ Amplifier Assembly	Digital Storage Adjustments Z Axis Adjustments Analog Deflection Adjustments	5-15 5-16 5-17
A7 Processor Assembly	None	
A8 Plug-In Power Supply Assembly	Low-Voltage Power Supply Adjustments	5-12
A9 Interface Assembly	None	
A10 HP-IB Interconnect Assembly	None	
A11 Primary Switching Assembly	None	
A12 Motherboard	None	
A13 Fan Module Assembly	None	
T1 Transformer Assembly	None	
U1 High-Voltage Multiplier Assembly	High-Voltage Power Supply Adjustments	5-13
V1 Cathode Ray Tube	High-Voltage Power Supply Adjustments Digital Storage Adjustments Z Axis Adjustments Analog Deflection Adjustments	5-13 5-15 5-16 5-17

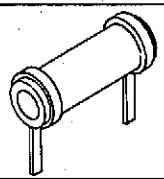
Table 5-3. HP 853A Factory-Selected Components

Reference Designator	Basis for Selection
A6R19	Selected in conjunction with A6R21 to center Y POSN adjustment.
A6R21	Selected in conjunction with A6R19 to center Y POSN adjustment.
A6R29	Selected to shift adjustment range of A6R30 Y GAIN.
A6R34	Selected in conjunction with A6R41 to center X POSN adjustment.
A6R41	Selected in conjunction with A6R34 to center X POSN adjustment.
A6R50	Selected to shift adjustment range of A6R20 X GAIN.

Table 5-4. HP Part Numbers of Standard Value Replacement Components (1 of 3)

CAPACITORS

RANGE: 1 to 24 pF
TYPE: Tubular
TOLERANCE:
1 to 9.1 pF = ±.25 pF
10 to 24 pF = ±5%



RANGE: 27 to 680 pF
TYPE: Dipped Mica
TOLERANCE: ±5%

Value (pF)	HP Part Number	C D
1.0	0160-2236	8
1.2	0160-2237	9
1.5	0150-0091	8
1.8	0160-2239	1
2.0	0160-2240	4
2.2	0160-2241	5
2.4	0160-2242	6
2.7	0160-2243	7
3.0	0160-2244	8
3.3	0150-0059	8
3.6	0160-2246	0
3.9	0160-2247	1
4.3	0160-2248	2
4.7	0160-2249	3
5.1	0160-2250	6
5.6	0160-2251	7
6.2	0160-2252	8
6.8	0160-2253	9
7.5	0160-2254	0
8.2	0160-2255	1
9.1	0160-2256	2
10.0	0160-2257	3
11.0	0160-2258	4
12.0	0160-2259	5
13.0	0160-2260	8
15.0	0160-2261	9
16.0	0160-2262	0
18.0	0160-2263	1
20.0	0160-2264	2
22.0	0160-2265	3
24.0	0160-2266	4

Value (pF)	HP Part Number	C D
27	0160-2306	3
30	0160-2199	2
33	0160-2150	5
36	0160-2308	5
39	0140-0190	7
43	0160-2200	6
47	0160-2307	4
51	0160-2201	7
56	0140-0191	8
62	0140-0205	5
68	0140-0192	9
75	0160-2202	8
82	0140-0193	0
91	0160-2203	9
100	0160-2204	0
110	0140-0194	1
120	0160-2205	1
130	0140-0195	2
150	0140-0196	3
160	0160-2206	2
180	0140-0197	4
200	0140-0198	5
220	0160-0134	1
240	0140-0199	6
270	0140-0210	2
300	0160-2207	3
330	0160-2208	4
360	0160-2209	5
390	0140-0200	0
430	0160-0939	4
470	0160-3533	0
510	0160-3534	1
560	0160-3535	2
620	0160-3536	3
680	0160-3537	4

Table 5-4. HP Part Numbers of Standard Value Replacement Components (2 of 3)

RESISTORS

RANGE: 10 to 464K Ohms
TYPE: Fixed-Film
WATTAGE: .125 at 125°C
TOLERANCE: ±1.0%

Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D
10.0	0757-0346	2	464	0698-0082	7	21.5K	0757-0199	3
11.0	0757-0378	0	511	0757-0416	7	23.7K	0698-3158	4
12.1	0757-0379	1	562	0757-0417	8	26.1K	0698-3159	5
13.3	0698-3427	0	619	0757-0418	9	28.7K	0698-3449	6
14.7	0698-3428	1	681	0757-0419	0	31.6K	0698-3160	8
16.2	0757-0382	6	750	0757-0420	3	34.8K	0757-0123	3
17.8	0757-0294	9	825	0757-0421	4	38.3K	0698-3161	9
19.6	0698-3429	2	909	0757-0422	5	42.2K	0698-3450	9
21.5	0698-3430	5	1.0K	0757-0280	3	46.4K	0698-3162	0
23.7	0698-3431	6	1.1K	0757-0424	7	51.1K	0757-0458	7
26.1	0698-3432	7	1.21K	0757-0274	5	56.2K	0757-0459	8
28.7	0698-3433	8	1.33K	0757-0317	7	61.9K	0757-0460	1
31.6	0757-0180	2	1.47K	0757-1094	9	68.1K	0757-0461	2
34.8	0698-3434	9	1.62K	0757-0428	1	75.0K	0757-0462	3
38.3	0698-3435	0	1.78K	0757-0278	9	82.5K	0757-0463	4
42.2	0757-0316	6	1.96K	0698-0083	8	90.9K	0757-0464	5
46.4	0698-4037	0	2.15K	0698-0084	9	100K	0757-0465	6
51.1	0757-0394	0	2.37K	0698-3150	6	110K	0757-0466	7
56.2	0757-0395	1	2.61K	0698-0085	0	121K	0757-0467	8
61.9	0757-0276	7	2.87K	0698-3151	7	133K	0698-3451	0
68.1	0757-0397	3	3.16K	0757-0279	0	147K	0698-3452	1
75.0	0757-0398	4	3.48K	0698-3152	8	162K	0757-0470	3
82.5	0757-0399	5	3.83K	0698-3153	9	178K	0698-3243	8
90.9	0757-0400	9	4.22K	0698-3154	0	196K	0698-3453	2
100	0757-0401	0	4.64K	0698-3155	1	215K	0698-3454	3
110	0757-0402	1	5.11K	0757-0438	3	237K	0698-3266	5
121	0757-0403	2	5.62K	0757-0200	7	261K	0698-3455	4
133	0698-3437	2	6.19K	0757-0290	5	287K	0698-3456	5
147	0698-3438	3	6.81K	0757-0439	4	316K	0698-3457	6
162	0757-0405	4	7.50K	0757-0440	7	348K	0698-3458	7
178	0698-3439	4	8.25K	0757-0441	8	383K	0698-3459	8
196	0698-3440	7	9.09K	0757-0288	1	422K	0698-3460	1
215	0698-3441	8	10.0K	0757-0442	9	464K	0698-3260	9
237	0698-3442	9	11.0K	0757-0443	0			
261	0698-3132	4	12.1K	0757-0444	1			
287	0698-3443	0	13.3K	0757-0289	2			
316	0698-3444	1	14.7K	0698-3156	2			
348	0698-3445	2	16.2K	0757-0447	4			
383	0698-3446	3	17.8K	0698-3136	8			
422	0698-3447	4	19.6K	0698-3157	3			

Table 5-4. HP Part Numbers of Standard Value Replacement Components (3 of 3)

RESISTORS

RANGE: 10 to 1.47M Ohms
TYPE: Fixed Film
WATTAGE: .5 at 125°C
TOLERANCE: ±1%

Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D
10.0	0757-0984	4	215	0698-3401	0	4.64K	0698-3348	4	110K	0757-0859	2
11.0	0575-0985	5	237	0698-3102	8	5.11K	0757-0833	2	121K	0757-0860	5
12.1	0757-0986	6	261	0757-1090	5	5.62K	0757-0834	3	133K	0757-0310	0
13.3	0757-0001	6	287	0757-1092	7	6.19K	0757-0196	0	147K	0698-3175	5
14.7	0698-3388	2	316	0698-3402	1	6.81K	0757-0835	4	162K	0757-0130	2
16.2	0757-0989	9	348	0698-3403	2	7.50K	0757-0836	5	178K	0757-0129	9
17.8	0698-3389	3	383	0698-3404	3	8.25K	0757-0837	6	196K	0757-0063	0
19.6	0698-3390	6	422	0698-3405	4	9.09K	0757-0838	7	215K	0757-0127	7
21.5	0698-3391	7	464	0698-0090	7	10.0K	0757-0839	8	237K	0698-3424	7
23.7	0698-3392	8	511	0757-0814	9	12.1K	0757-0841	2	261K	0757-0064	1
26.1	0757-0003	8	562	0757-0815	0	13.3K	0698-3413	4	287K	0757-0154	0
28.7	0698-3393	9	619	0757-0158	4	14.7K	0698-3414	5	316K	0698-3425	8
31.6	0698-3394	0	681	0757-0816	1	16.2K	0757-0844	5	348K	0757-0195	9
34.8	0698-3395	1	750	0757-0817	2	17.8K	0698-0025	8	383K	0757-0133	5
38.3	0698-3396	2	825	0757-0818	3	19.6K	0698-3415	6	422K	0757-0134	6
42.2	0698-3397	3	909	0757-0819	4	21.5K	0698-3416	7	464K	0698-3426	9
46.4	0698-3398	4	1.00K	0757-0159	5	23.7K	0698-3417	8	511K	0757-0135	7
51.1	0757-1000	7	1.10K	0757-0820	7	26.1K	0698-3418	9	562K	0757-0868	3
56.2	0757-1001	8	1.21K	0757-0821	8	28.7K	0698-3103	9	619K	0757-0136	8
61.9	0757-1002	9	1.33K	0698-3406	5	31.6K	0698-3419	0	681K	0757-0869	4
68.1	0757-0794	4	1.47K	0757-1078	9	34.8K	0698-3420	3	750K	0757-0137	9
75.0	0757-0795	5	1.62K	0757-0873	0	38.3K	0698-3421	4	825K	0757-0870	7
82.5	0757-0796	6	1.78K	0698-0089	4	42.2K	0698-3422	5	909K	0757-0138	0
90.0	0757-0797	7	1.96K	0698-3407	6	46.4K	0698-3423	6	1M	0757-0059	4
100	0757-0198	2	2.15K	0698-3408	7	51.1K	0757-0853	6	1.1M	0757-0139	1
110	0757-0798	8	2.37K	0698-3409	8	56.2K	0757-0854	7	1.21M	0757-0871	8
121	0757-0799	9	2.61K	0698-0024	7	61.9K	0757-0309	7	1.33M	0757-0194	8
133	0698-3399	5	2.87K	0698-3101	7	68.1K	0757-0855	8	1.47M	0698-3464	5
147	0698-3400	9	3.16K	0698-3410	1	75.0K	0757-0856	9			
162	0757-0802	5	3.48K	0698-3411	2	82.5K	0757-0857	0			
178	0698-3334	8	3.83K	0698-3412	3	90.9K	0757-0858	1			
196	0757-1060	9	4.22K	0698-3346	2	100K	0757-0367	7			

ADJUSTMENTS

5-12. LOW-VOLTAGE POWER SUPPLIES CHECK AND ADJUSTMENT

REFERENCE:

A3 and A8 Schematics

DESCRIPTION:

The low-voltage supplies on Plug-in Power Supply Assembly A8 and on Display Power Supply A3 are checked and adjusted as necessary for correct output voltage levels.

EQUIPMENT:

Digital Voltmeter	HP 3455A
Spectrum Analyzer plug-in	HP 8557A, 8558B, or 8559A

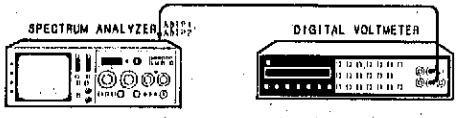


Figure 5-1. Low-Voltage Power Supplies Adjustment Test Setup

PROCEDURE:

Plug-In Power Supply Assembly A8

1. Set display LINE switch to OFF, disconnect ac power cord, and remove the HP 853A top cover. Connect the equipment as shown in Figure 5-1.

NOTE

Connect digital voltmeter ground to test point A8TP2 when monitoring voltages on Plug-In Power Supply Assembly A8.

2. Reconnect ac power cord, install spectrum analyzer plug-in, and set display LINE switch to ON.

3. Adjust potentiometer A8R13 (+15.05V ADJ) for +15.05 ±.01 Vdc at A8TP1.

4. Connect digital voltmeter to A8TP5. Adjust potentiometer A8R17 (−12.65V ADJ) for a voltmeter reading of −12.65 ±0.01 Vdc.

5-12. LOW-VOLTAGE POWER SUPPLIES CHECK AND ADJUSTMENT (Cont'd)

WARNING

The voltage at A8TP4 (check in the next step) is hazardous.

5. Connect digital voltmeter to A8TP4. Voltmeter should indicate + 100 ±2 Vdc.

6. Disconnect the digital voltmeter. The three amber LEDs (DS1 through DS3) on Plug-In Power Supply Assembly A8 should be lit, indicating that the supply voltages are present and at the correct levels.

7. Set LINE switch to OFF and remove spectrum analyzer plug-in from the display mainframe.

8. Set LINE switch to ON. The + 100V power indicator LED (DS1) on Plug-In Power Supply Assembly A8 should be very dimly lit, indicating proper safety shutdown of the + 100V supply when plug-in spectrum analyzer is removed from display mainframe. (Shutdown is partial; 100V supply output is reduced to less than 20 volts.)

Display Power Supply Assembly A3

9. Set LINE switch to OFF and install spectrum analyzer plug-in in display mainframe. Set LINE switch to ON.

NOTE

When measuring voltages on Display Power Supply Assembly A3, connect digital voltmeter ground to test point A3TP5.

10. Connect digital voltmeter to test point A3TP2. Adjust potentiometer A3R20 (+ 15V ADJ) for a voltmeter reading of + 15.00 ±0.01 Vdc.

11. Connect digital voltmeter to test point A3TP4. Adjust potentiometer A3R21 (− 15V ADJ) for a voltmeter reading of − 15.00 ±0.01 Vdc.

12. Connect digital voltmeter to test point A3TP7. Adjust potentiometer A3R28 (+ 5V ADJ) for a voltmeter reading of + 5.05 ±0.01 Vdc.

13. Connect digital voltmeter to test point A3TP3. Voltmeter should indicate − 12.0 ±0.5 Vdc.

WARNING

The voltage at test point A3TP6 (checked in the next step) is high enough to cause you severe injury if contacted.

14. Connect the digital voltmeter to test point A3TP6. Voltmeter should indicate + 158 ±2.0 Vdc.

15. Disconnect the digital voltmeter. The four amber LEDs (DS1 through DS4) on Display Power Supply Assembly A3 should be lit, indicating that the supply voltages are present and at the correct levels.

16. When you have completed the above checks and adjustments, set the LINE to OFF, disconnect the ac power cord, and replace the HP 853A top cover.

5-13. HIGH VOLTAGE POWER SUPPLY ADJUSTMENT

REFERENCE:

A4 Schematic. See Figure 5-11 at the back of this section for locations of adjustments on assemblies A5 and A6.

DESCRIPTION:

A high-voltage probe is required to measure the high-voltage cathode supply to the CRT. The probe accuracy is checked by comparing measurements of the +158V supply with, and without, the probe in the test setup. Any error is compensated for when the CRT cathode supply voltage is set. The Intensity Limit adjustment is set to limit the CRT control grid voltage and, in effect, to limit the maximum CRT trace intensity.

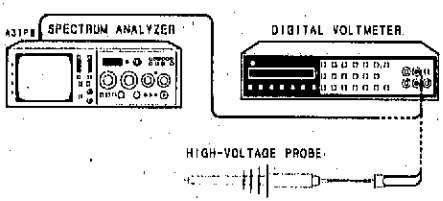


Figure 5-2. High-Voltage Power Supply Adjustment Test Setup

EQUIPMENT:

Digital Voltmeter	HP 3455A
High-Voltage Probe (1000:1 Divider)	HP 34111A
Spectrum Analyzer plug-in	HP 8559A, 8558B, or 8557A

WARNING

To minimize shock hazard, use a non-metallic adjustment tool for adjustments on High Voltage Power Supply Assembly A4.

WARNING

The following procedure probes voltages that, if contacted, could cause personal injury or death.

NOTE

Adjustment of High Voltage Power Supply Assembly A4 should not be a routine maintenance procedure. Adjustment should be done only when the high-voltage power supply or the CRT is repaired or replaced.

5-13. HIGH VOLTAGE POWER SUPPLY ADJUSTMENT (Cont'd)

NOTE

If High Voltage Power Supply Assembly A4, or an adjustable component in the assembly, is replaced, set all adjustments on the replaced assembly to midrange (except A4R18 INT LIM, which should be set fully counterclockwise) before turning the instrument on. If the CRT is replaced, set the front-panel INTENSITY control fully counterclockwise before applying power.

PROCEDURE:

WARNING

After disconnecting the ac line power cord, allow at least 30 seconds for capacitors in the high-voltage power supply to discharge before removing the protective cover of High Voltage Power Supply Assembly A4.

1. Set LINE switch OFF, disconnect power cord, and remove the HP 853A top cover. Remove protective cover of High Voltage Power Supply Assembly A4.

2. Remove screw that attaches assembly A4 to cavity. Partly remove board from cavity to read value of voltage written on Transformer Assembly A4A1. Record this voltage and reattach assembly A4 to cavity with screw.

_____ Vdc

CAUTION

To prevent permanent damage to the CRT, be prepared to turn off the instrument if a bright spot appears on screen. Set INT LIM adjustment A4R18 fully counterclockwise before installing a new High Voltage Power Supply Assembly A4.

3. Reconnect power cord, install spectrum analyzer plug-in, and set LINE switch ON. If a bright spot appears on screen, immediately turn off display mainframe. If bright spot does not appear, set controls as follows:

TRACE A	STORE BLANK
TRACE B	STORE BLANK
DGTL AVG	OFF
INPUT – B→A	OFF
SCALE	Full counterclockwise
INTEN	Dim CRT trace
FOCUS	Midrange
FREQ SPAN/DIV	0 MHz
RESOLUTION BW	3 MHz
INPUT ATTEN	10 dB
REFERENCE LEVEL	– 10 dBm
Amplitude Scale	LIN
SWEEP TIME/DIV	MAN
VIDEO FILTER	MAX (detent)

5-13. HIGH VOLTAGE POWER SUPPLY ADJUSTMENT (Cont'd)

High Voltage Power Supply

4. Calibrate high-voltage probe as follows:

   a. Set digital voltmeter (DVM) to AUTO range, measure output of +158V supply at A3TP6 with standard DVM probe, and record reading.

   +_____Vdc

   b. Connect 1000:1 divider probe to DVM, measure +158V supply, and record reading.

   +_____Vdc

   c. Divide reading recorded in step 4a into reading recorded in step 4b. This gives calibration factor of high-voltage probe.

   calibration factor_____

   d. Multiply voltage recorded in step 2 by calibration factor calculated in step 4c to yield desired voltage reading.

   –_____Vdc

WARNING

High voltage present at A4TP1 could, if contacted, cause severe injury or death.

5. Set DVM to 10V range and attach high-voltage probe ground lead to the HP 853A chassis. Measure output of high-voltage cathode power supply at A4TP1 CATH test hole (plated-through hole at edge of P.C. board).

6. Adjust A4R4 HV for a voltmeter reading equal to the voltage reading calculated in step 4d.

Intensity Limit and Focus Limit

NOTE

The DVM must have 10 megohms input resistance for correct measurement. If the HP 3455A Digital Voltmeter is used, the 100-volt or the 1000-volt range must be used. Do not use AUTO range.

7. Disconnect 1000:1 divider probe from DVM and connect standard DVM probe. Connect DVM to CONT GATE OUT test point A6TP2.

5-13. HIGH VOLTAGE POWER SUPPLY ADJUSTMENT (Cont'd)

8. Set front-panel INTEN control for a voltage reading of 30.0 ±0.2V. (If voltage at CONT GATE OUT test point A6TP2 cannot be reduced to +30V, adjust MIN INTEN A6R153 just enough to allow reading of +30 ±0.2V.)

CAUTION

This voltage must be set correctly before INT LIM potentiometer A4R18 is adjusted, or permanent damage to the CRT could result.

9. Adjust MAN SWEEP control to midrange position.

10. Adjust A4R18 INT LIM clockwise until a dot is barely visible on CRT.

11. Adjust front-panel INTEN control to display CRT dot at normal intensity. Adjust A4R29 FOCUS LIMIT for best focus of CRT dot.

12. Repeat steps 8–11 until no further adjustment is necessary.

13. Disconnect DVM from test point A6TP2. Set LINE switch OFF, disconnect power cord, and wait at least 30 seconds before replacing protective cover of High Voltage Power Supply Assembly A4.

14. Perform Z-Axis Adjustment Procedure (paragraph 5-16 in this section).

5-14. DIGITAL STORAGE TEST ROUTINES

Eleven test routines, contained in the firmware of the HP 853A, are used to adjust, verify the correct operation of, and troubleshoot the digital storage circuitry.

Test routines are accessed by turning the instrument off, pressing and holding PLOT GRAT, turning the instrument on, and then releasing PLOT GRAT. The first routine accessed in this manner will be test routine #0.

In test routines #0 and 4, a four-character code, displayed on the right-hand side of the CRT, represents the current revision of the program ROM.

The test routines are numbered from #0 through #9 and #A on the left-hand side of the CRT. To view the output of the various test routines, proceed as follows:

1. Access test routine #0 in the manner described above.
2. After test routine #0 is selected, the PLOT GRAT push button can be pressed and released successively to step the test routines sequentially from #1 through #A.
3. For all test modes, selecting STORE BLANK A and STORE BLANK B at the same time switches the display to the analog mode. Although this doesn't deactivate the test routines, they will no longer be visible on the CRT. For any other TRACE A or TRACE B selection, the test routine display is active.
4. To exit the test routine mode, press and release PLOT GRAT and PLOT TRACE simultaneously, or turn the instrument LINE power switch OFF then ON.

Display Adjust Line Test Pattern

Use test routine #0 (Figure 5-3) for the following front panel adjustments:

TRACE ALIGN
X POSN
Y POSN

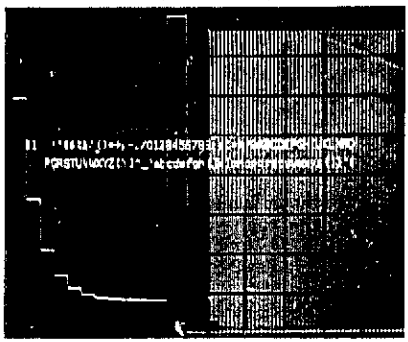
NOTE

The slightly different display pattern of test routine #4 can also be used for these adjustments.

The trace is generated from fixed values in memory that correspond to the top horizontal graticule line and the vertical centerline. When trace alignment and position adjustments are properly made, the generated horizontal line should be displayed over the top horizontal graticule line, and the center tick mark should be positioned over the vertical centerline etched on the CRT. This matches the center of the top horizontal graticule line with the corresponding position sent through the Hewlett-Packard Interface Bus (HP-IB) to the plotter.

5-14. DIGITAL STORAGE TEST ROUTINES (Cont'd)

Test Routine #0



Test Routine #1

Figure 5-3. Test Routines #0 and #1

Stroke Generator Test Pattern

Test routine #1 (Figure 5-3) is used for the following adjustments:

INTEN EQ (A5R104)
Y FB (A5R99)
STRK GAIN (A5R97)

The character display verifies operation of the character ROM and associated circuitry. The full ASCII character set is displayed.

The stairstep display verifies operation of the output digital-to-analog converter (DAC). Eleven levels should be seen; these correspond to 512, 256, 128, 64, 32, 16, 8, 4, 2, 1, and 0. The transitions to the last two levels are difficult to see on the CRT trace. Note that the levels have been offset by 128 to position all of them within the graticule area.

The square wave is used to adjust and verify the operation of the stroke generator; there should be no more than a minimal overshoot or undershoot. Note that the overshoot or undershoot appears at the right-hand edge of the square wave rather than at the usual left-hand edge. This is because the CRT traces are written backward (going from right to left).

The test pattern on the right half of the screen is used to adjust and verify the stroke intensity modulation circuitry. When the front-panel INTEN control is at midrange, the brightness of the short strokes (the inverted 'V') should be the same as that of the rest of the pattern.

5-14. DIGITAL STORAGE TEST ROUTINES (Cont'd)

Test Routine #2

Test Routine #3

Figure 5-4. Test Routines #2 and #3

Peak Detector Droop Test

Test routine #2 (Figure 5-4) is used to measure the amount of hold-mode droop in the maximum peak detector circuit. The droop is the amount the voltage on the hold capacitor decreases over time because of leakage of the hold capacitor and of the components connected to this capacitor. The firmware implements a digital-storage oscilloscope mode. The sweep is triggered by a positive-going signal at the horizontal center of the screen. The sweep time per division is adjustable with the spectrum analyzer SWEEP TIME/DIV control. Note that only the right half of the screen is used for the test mode. Trace A displays the data acquired by the sample detector, while Trace B displays the data acquired by the maximum peak detector.

Focus Test Pattern

Test routine #3 (Figure 5-4) is used for the following adjustments:

FOCUS (Front panel)
HF TRIM (A6C61)
ASTIG (A3R30)
HF GAIN (A6R151)
DYN FOCUS (A6R135)
FOCUS LIMIT (A4R29)

The separate dots making up the letter X should be observed to determine how well the CRT beam is focused. The characters can also be moved to mid-screen and bottom-screen positions to check the focus in those areas of the screen by momentarily pressing PLOT TRACE.

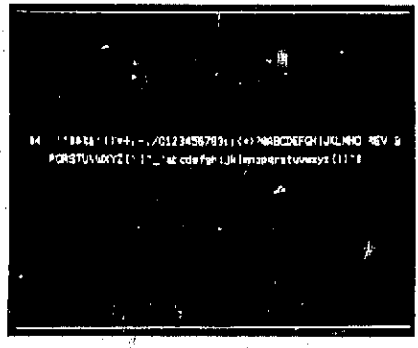
5-14. DIGITAL STORAGE TEST ROUTINES (Cont'd)

Output Test Pattern

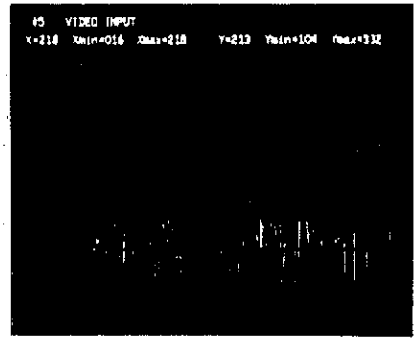
Test routine #4 (Figure 5-5) provides the output test pattern that is used for the following adjustments:

TRACE ALIGN (Front panel)
X POSN (Front panel)
Y POSN (Front panel)
PATT (A3R31)
DGTL X GAIN (A5R81)
DGTL X OFFSET (A5R92)
DGTL Y OFFSET (A6R2)
DGTL Y GAIN (A6R4)

The lines are generated from fixed values in memory that correspond to the top, bottom, left, and right graticule lines that are transmitted over the HP-IB to a plotter. The generated horizontal lines should coincide with the top and bottom graticule lines etched on the CRT. The two vertical lines should be spaced 10 divisions apart, but are often offset slightly from the side graticule lines because of CRT nonlinearities. (X POSN is adjusted so that the center tick mark lines up with the center vertical graticule line.)



Test Routine #4



Test Routine #5

Figure 5-5. Test Routines #4 and #5

Input Test Routine

Test routine #5 (Figure 5-5) is used for the following adjustments:

MAX OFF (A5R1)
MIN OFF (A5R25)
ADC OFF (A5R58)
ADC GAIN (A5R71)
SWP OFF (A5R50)
SWP GAIN (A5R52)

5-14. DIGITAL STORAGE TEST ROUTINES (Cont'd)

The trace data is acquired using an algorithm similar to that used for normal operation, except that absolute rather than incremented X positions are used. To avoid gaps in the trace, use sweep times of 100 ms per division or slower. When manual sweep mode is used, the trace may be updated in either direction. The PLOT TRACE push button can be pressed to switch between three ADC input signals: the maximum peak detector output, the minimum peak detector output, and the video signal from the spectrum analyzer plug-in. The following information is displayed:

X: Instantaneous value of X

Xmin: Minimum value of sweep, updated at retrace

Xmax: Maximum value of sweep, updated at retrace

Y: Instantaneous value of Y (the selected input)

Ymin: Minimum value of the selected input, updated at retrace

Ymax: Maximum value of the selected input, updated at retrace

The readings are used primarily to set the gain and offset adjustment of sweep (X) and video (Y), preceding the analog-to-digital conversion.

No gaps in the trace should be seen when a horizontal line is displayed in linear mode with sweep times of 100 ms per division and slower. If there are gaps, the digital-to-analog converter (DAC) used in the ADC circuit is the primary suspect.

Sweep Time Test

Test routine #6 measures the sweep time of the spectrum analyzer plug-in by measuring the time between retrace pulses. Momentarily pressing the PLOT TRACE push button clears the timing and triggers a new sweep. If the analog display mode is selected, an analog trace is displayed during each sweep, after which the display mainframe switches to the digital mode to display the measured sweep time.

Memory Test Routines

Test routines #7, #8, and #9 perform tests on the various memories that are accessed by the microprocessor. The memory is repeatedly tested as long as the instrument is in a given test routine. This provides a convenient means to troubleshoot intermittent memory problems.

For example, run the test unattended for an extended length of time, or try heating, cooling, or shaking the microprocessor board (Processor Assembly A7). If a failure occurs, the test stops, and failure indicators are displayed on the CRT. The indicators are a horizontal line at a given position on the CRT and repeated characters in the annotation area of the CRT. These indicators assist in narrowing the fault location to a defective IC. (See Memory Fault Location Indicators listed in Table 5-5 below.) If two indicators point to different faults, start with the primary indicator given in the table.

When the instrument is turned on, a power-on verification test is performed. This test runs each of the memory test routines once and takes about 5 seconds to complete. If the verification test fails, refer to Table 5-5 for an interpretation of the displayed failure indicators.

5-14. DIGITAL STORAGE TEST ROUTINES (Cont'd)

System Memory Test. Select test routine #7 to test system memory. Any failure that affects the data bus also shows up as a failure in this test. Since the character memory area is located in the system memory, a pattern is seen moving through the annotation area of the CRT. Unlike the other test routines, the test routine label ("#7") is not displayed during test routine #7. If the test stops, refer to the Memory Fault Location Table for an interpretation of the displayed failure indicators.

Program Memory Test. Select test routine #8 to test program memory. No trace or character, except for '#8,' is displayed unless the test fails. Refer to the Memory Fault Location Table for an interpretation of displayed failure indicators.

Stroke Memory Test. Select test routine #9 to test stroke (trace) memory. A momentary display of '#9' is followed by an unfocused pattern moving through the entire CRT area. If the test fails, refer to the Memory Fault Location Table for an interpretation of displayed failure indicators. Each cycle through the test takes about 4 seconds.

Table 5-5. Memory Fault Location Indicators

Primary Indicator	Secondary Indicator	Circuit Under Test	Defective IC	Test Routine Number
Line at 0 dB	Letter A	System Memory	*	#7
Line at –5 dB	Letter B	System Memory	A7U6	#7
Line at –10 dB	Letter C	System Memory	A7U7	#7
Letter D	Line at –15 dB	Program ROM	A7U34	#8
Letter E	Line at –20 dB	Stroke Memory	A7U8	#9
Letter F	Line at –25 dB	Stroke Memory	A7U9	#9
Letter G	Line at –30 dB	Stroke Memory	A7U10	#9
Letter H	Line at –35 dB	Stroke Memory	A7U11	#9

*Any failure that affects both high and low nibbles of data on data bus can cause this failure.

HP-IB Test.

To check the HP-IB hardware, select test routine #A. In this routine, the HP-IB processor is set to a Talk-Only/Listen-Only mode, which allows it to handshake and talk to itself to perform a self-test. Additionally, the processor sends a binary count pattern out on the HP-IB connector and activates the HP-IB handshake lines. With an oscilloscope, you can quickly check these outputs for evidence of problems in the associated bus driver circuitry.

The test routine displays "#A" if the HP-IB hardware is working properly, and "FAILED" if it is not. Momentarily pressing the PLOT TRACE push button clears the "FAILED" display and restarts the test, each cycle of which takes about 0.1 second.

5-17. ANALOG DEFLECTION ADJUSTMENTS (Cont'd)

5-15. DIGITAL STORAGE ADJUSTMENTS

REFERENCE:

A5 and A6 Schematics. See Figure 5-11 at the back of this section for location of adjustments on assemblies A5 and A6.

NOTE

The analog deflection adjustments (paragraph 5-17) must be performed before the digital storage adjustments. Each of the digital storage adjustments must be performed in the order presented.

DESCRIPTION:

A description of all digital storage test routines is provided in paragraph 5-14, with instructions for entering and exiting the routines. For convenience, some descriptions are repeated here. The test setup for digital storage adjustments is shown in Figure 5-6.

The following adjustments are included under Digital Storage Adjustments:

Digital-to-Analog Output Adjustments

- Stroke Generator Adjustments
- Digital Gain and Offset Adjustments

Analog-to-Digital Input Adjustments

- Peak Detector Droop Test
- ADC, Peak Detector, and Sweep Adjustments

EQUIPMENT:

Required equipment is listed individually for each adjustment section.

PROCEDURE:

Remove top and bottom covers from HP 853A. Perform the following adjustment procedures and tests in the order they are presented.

Stroke Generator Adjustments

DESCRIPTION:

Test routine #1 is used to adjust and verify correct operation of the stroke generator circuitry. The character display verifies operation of the character ROM and associated circuitry. The full ASCII character set is displayed.

The stairstep display verifies response of the output digital-to-analog converter (DAC) to changes in each of its 10 input bits. Eleven levels should be seen; these correspond to 512, 256, 128, 64, 32, 16, 8, 4, 2, 1, and 0. The

ADJUSTMENTS

5-15. DIGITAL STORAGE ADJUSTMENTS (Cont'd)

transitions to the last two levels are difficult to see on the CRT trace. Note that the levels have been offset by 128 to position all of them within the graticule area for convenient viewing.

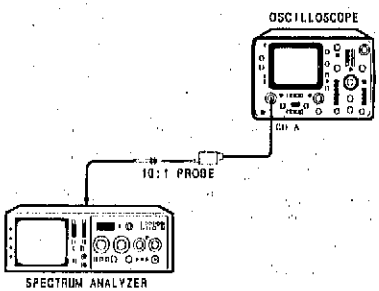


Figure 5-6. Stroke Generator Adjustments Test Setup

The square wave display (adjacent to the stairstep) is used to adjust the stroke generator circuitry; there should be no more than a minimal overshoot or undershoot. Note that the overshoot or undershoot appears at the right-hand edge of the square wave rather than at the usual left-hand edge. This is because the CRT traces are written backward (going from right to left).

EQUIPMENT:

Oscilloscope	HP 1741A
10:1 Divider Probe	HP 10004D
Spectrum Analyzer plug-in	HP 8559A, 8558B, or 8557A

PROCEDURE:

1. Set controls as follows:

HP 853A and Spectrum Analyzer plug-in:

TRACE A	WRITE
TRACE B	STORE BLANK
DGTL AVG	OFF
INP – B↦A	OFF
SCALE	Full counterclockwise
INTEN	Midrange
FREQ SPAN/DIV	0 MHz
RESOLUTION BW	3 MHz
INPUT ATTEN	10 dB
REFERENCE LEVEL	–10 dBm
Amplitude Scale	LIN
SWEEP TIME/DIV	AUTO
SWEEP TRIGGER	FREE RUN

5-15. DIGITAL STORAGE ADJUSTMENTS (Cont'd)

HP 1741A:

Channel A Volts/DIV ..... 0.1V (1.0V/DIV on screen)
TIME/DIV ..... 0.5 msec

2. Simultaneously press PLOT GRAT and LINE push buttons to turn the instrument on and display test routine #0. Press PLOT GRAT again to select test routine #1.

3. Connect oscilloscope probe to A5TP3 STROKE LEN and probe ground to A5TP1 GND. Adjust TRIGGER control as necessary for a stable display on the oscilloscope CRT similar to that shown in Figure 5-7.

4. Adjust A5R99 Y FB potentiometer for a flat-topped stroke pattern (far right pattern on the HP 853A CRT). Corresponding V-pattern on oscilloscope CRT should also appear flat-topped after adjustment (see Figure 5-7).

5. Adjust A5R97 STRK GAIN potentiometer for a symmetrical V-pattern on oscilloscope CRT.

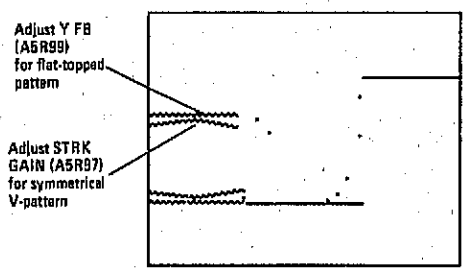


Figure 5-7. Stroke Generator Pattern

6. Repeat steps 4 and 5 until no further adjustment is necessary.

7. Disconnect oscilloscope from A5TP3.

8. Verify that all characters are clearly and correctly displayed on CRT.

9. Verify that there are 11 levels on the staircase displayed in test routine #1. (The last two transitions are difficult to discern.)

10. Observe stroke pattern on the HP 853A CRT. With INTEN control at midrange setting, adjust A5R104 INTEN EQ potentiometer for uniform intensity above and below inverted 'V.'

5-15. DIGITAL STORAGE ADJUSTMENTS (Cont'd)

Digital Gain and Offset Adjustments

DESCRIPTION:

The digital gain and offset adjustments are performed after the analog deflection adjustments. The digital gain and offset adjustments align the digital reference pattern of test routine #4 with the fixed CRT graticule lines. This establishes a digital X and Y coordinate for each point on the CRT, and ensures that CRT plots made via HP-IB correspond to the CRT display.

EQUIPMENT:

Spectrum Analyzer plug-in	HP 8559A, 8558B, or 8557A

PROCEDURE:

1. Set controls as follows:

TRACE A	WRITE
TRACE B	STORE BLANK
DGTL AVG	OFF
INPUT – B→A	OFF
SCALE	Full counterclockwise
INTEN	Midrange
SWEEP TIME/DIV	AUTO
SWEEP TRIGGER	FREE RUN

2. Simultaneously press PLOT GRAT and LINE switch to turn instrument on and display test routine #0. Press PLOT GRAT to select test routine #4.

3. Adjust A5R81 DGTL X GAIN and A5R92 DGTL X OFFSET so that two vertical lines of test pattern coincide with extreme left and right graticule lines on CRT. Exact coincidence should occur at center of both graticule lines. These two adjustments are interactive; repeat until best match is achieved.

4. Readjust A5R92 DGTL X OFFSET so that tick mark at center of display coincides with center graticule line.

5. Adjust A6R4 DGTL Y GAIN and A6R2 DGTL Y OFFSET so that two horizontal lines of test pattern coincide with top and bottom graticule lines on CRT. Exact coincidence should occur at center of both graticule lines. These two adjustments are interactive; repeat until best match is achieved.

Peak Detector Droop Test

DESCRIPTION:

Test routine #2 is used to measure the amount of hold-mode droop in the maximum peak detector circuit. The droop is the amount the voltage on the hold capacitor decreases over time because of leakage of the hold

5-15. DIGITAL STORAGE ADJUSTMENTS (Cont'd)

capacitor and of the components connected to this capacitor. The firmware implements a digital-storage oscilloscope mode. The sweep is triggered by a positive-going signal at the horizontal center of the screen. The sweep time per division is adjustable with the spectrum analyzer SWEEP TIME/DIV control. Note that only the right half of the screen is used for the test mode. Trace A displays the data acquired by the sample detector, while Trace B displays the data acquired by the maximum peak detector.

EQUIPMENT:

Spectrum Analyzer plug-in	HP 8559A, 8558B, or 8557A

PROCEDURE:

1. Set controls as follows:

TRACE A	STORE BLANK
TRACE B	STORE BLANK
DGTL AVG	OFF
INPUT – B→A	OFF
SCALE	Full counterclockwise
INTEN	Midrange
FREQ SPAN/DIV	5 MHz
RESOLUTION BW	100 kHz
INPUT ATTEN	10 dB
Amplitude Scale	LIN
SWEEP TIME/DIV	0.1 mSEC
SWEEP TRIGGER	FREE RUN

2. Connect CAL OUTPUT signal to spectrum analyzer INPUT. Adjust REFERENCE LEVEL and TUNING controls to power level and frequency indicated on front panel next to CAL OUTPUT connector, placing signal peak at top graticule line in center of CRT.

3. Set TRACE A to WRITE, and set LINE switch OFF.

4. Jumper test point A5TP15 POS PEAK TEST to chassis ground. (See Figure 5-11 for location of A5TP15.)

5. Simultaneously press PLOT GRAT and LINE switch to turn instrument on and display test routine #0. Press PLOT GRAT two more times to select test routine #2.

6. Set spectrum analyzer SWEEP TIME/DIV to 0.5 sec. and observe droop waveform on right side of CRT. Decay of signal level from top screen should be less than 8 vertical divisions (full screen) within two horizontal divisions (1 sec.).

7. Remove jumper from A5TP15.

ADC, Peak Detector, and Sweep Adjustments

DESCRIPTION:

Offset adjustments for the maximum and minimum peak detector circuitry are provided to minimize differences between the peak detector output levels and a fixed video input level.

5-15. DIGITAL STORAGE ADJUSTMENTS (Cont'd)

The offset and gain of the ADC are adjusted for accurate digitizing of the video input signal from the spectrum analyzer plug-in. Y values of 48 and 848 correspond to the bottom and top CRT graticule lines respectively.

The horizontal sweep ramp from the spectrum analyzer plug-in is scaled and shifted by the sweep offset and gain adjustments. This sweep ramp is digitized to determine the horizontal calibration of the digitized video data. X values of 16 and 496 correspond to the leftmost and rightmost CRT graticule lines respectively (i.e., the beginning and end of the sweep ramp).

EQUIPMENT:

Digital Voltmeter	HP 3455A
Spectrum Analyzer plug-in	HP 8559A, 8558B, or 8557A

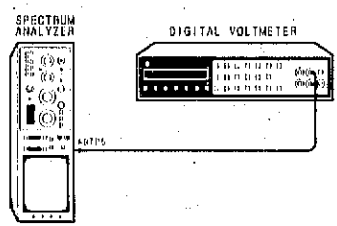


Figure 5-8. ADC, Peak Detector and Sweep Adjustments Test Setup

PROCEDURE:

Peak Detector Offsets

1. Set controls as follows:

TRACE A	WRITE
TRACE B	WRITE
DGTL AVG	OFF
INPUT – B→A	OFF
SCALE	Full counterclockwise
INTEN	Midrange
TUNING	>30 MHz
FREQ SPAN/DIV	0 MHz
RESOLUTION BW	3 MHz
INPUT ATTEN	10 dB
REFERENCE LEVEL	– 10 dBm
Amplitude Scale	LIN
SWEEP TIME/DIV	MAN
SWEEP TRIGGER	FREE RUN
VIDEO FILTER	MAX (detent)
MANUAL SWEEP	Midrange

5-15. DIGITAL STORAGE ADJUSTMENTS (Cont'd)

NOTE

Tolerance for all adjustments is ±1 count.

2. Simultaneously press PLOT GRAT and LINE switch to turn instrument on and display test routine #0.

3. Press PLOT GRAT to select test routine #5. Note that pressing PLOT TRACE selects the video input signal, the output of the maximum peak detector circuit, or the output of the minimum peak detector circuit as the input to the ADC. Select VIDEO INPUT.

4. Connect CAL OUTPUT signal to spectrum analyzer INPUT. Adjust REFERENCE LEVEL and TUNING controls to power level and frequency indicated on front panel next to CAL OUTPUT connector.

5. Adjust spectrum analyzer TUNING control for a maximum value of Y displayed on the display mainframe CRT (i.e., tune to peak of CAL OUTPUT signal).

6. Adjust spectrum analyzer REFERENCE LEVEL control for Y = 448 on the CRT.

7. Press PLOT TRACE to select MAX PEAK DET as the ADC input.

8. Adjust MAX OFF potentiometer A5R1 for Y = 448 on the CRT.

9. Press PLOT TRACE to select MIN PEAK DET as the ADC input.

10. Adjust MIN OFF potentiometer A5R25 for Y = 448 on the CRT.

11. Press PLOT TRACE to select VIDEO INPUT. Repeat steps 5 – 11 at least once until no further adjustment is necessary.

ADC Offset and Gain

NOTE

This adjustment directly affects relative vertical trace positioning between ANALOG DISPLAY and DIGITAL DISPLAY modes.

12. Disconnect CAL OUTPUT signal from spectrum analyzer INPUT. Set INTEN control full counterclockwise.

13. Select ANALOG DISPLAY mode by setting TRACE A and TRACE B to STORE BLANK. Increase INTEN control setting until dot is visible on CRT.

14. Adjust spectrum analyzer VERTICAL POSN and MANUAL SWEEP controls to place dot precisely on center of bottom CRT graticule line.

5-15. DIGITAL STORAGE ADJUSTMENTS (Cont'd)

15. Set TRACE A to WRITE and increase INTEN control setting as necessary to display test routine #5. Adjust ADC OFF potentiometer A5R58 for Y = 048 on the CRT.

16. Set INTEN control full counterclockwise.

17. Set TRACE A to STORE BLANK to select ANALOG DISPLAY mode. Increase INTEN control setting until dot is visible on CRT.

18. Connect CAL OUTPUT signal to spectrum analyzer INPUT. Adjust spectrum analyzer TUNING control to place dot as close as possible to top of CRT (i.e., tune to peak of CAL OUTPUT signal).

19. Adjust spectrum analyzer REFERENCE LEVEL control to place dot precisely on top CRT graticule line.

20. Set TRACE A to WRITE and increase INTEN control setting as necessary to display test routine #5. Adjust ADC GAIN potentiometer A5R71 for Y = 848 on the CRT.

21. Repeat steps 12 – 20 at least once until no further adjustment is necessary.

Sweep Offset and Gain

NOTE

This adjustment directly affects relative horizontal trace positioning between ANALOG DISPLAY and DIGITAL DISPLAY modes.

22. Connect digital voltmeter to A9TP5, as shown in Figure 5-8.

23. Adjust spectrum analyzer MANUAL SWEEP control for −5.00 ±0.01 Vdc at A9TP5.

24. Adjust SWP OFF (sweep offset) potentiometer A5R50 for X = 016 on the CRT.

25. Adjust spectrum analyzer MANUAL SWEEP control for +5.00 ±0.01 Vdc at A9TP5.

26. Adjust SWP GAIN potentiometer A5R52 for X = 496 on the CRT.

27. Repeat steps 22 – 26 at least once until no further adjustment is necessary.

ADJUSTMENTS

5-16. Z AXIS ADJUSTMENTS

REFERENCE:

A3, A4, and A6 Schematics. See Figure 5-11 at the back of this section for locations of adjustments on assemblies A5 and A6.

DESCRIPTION:

Internal test routines of the display mainframe are used to adjust its astigmatism, dynamic focus, trace alignment, and frequency response.

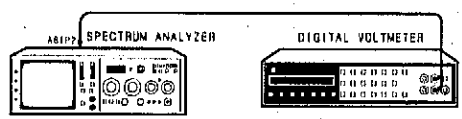


Figure 5-9. Z Axis Adjustment Test Setup

EQUIPMENT:

Spectrum Analyzer plug-in	HP 8559A, 8558B, or 8557A
Digital Voltmeter	HP 3455A

PROCEDURE:

WARNING

To minimize shock hazard, use a non-metallic adjustment tool for adjustments on XYZ Amplifier Assembly A6.

Focus Limit, Astigmatism, and Dynamic Focus

1. Set LINE switch OFF, disconnect power cord and remove HP 853A top cover.
2. Reconnect power cord and install spectrum analyzer plug-in.
3. Set display mainframe controls as follows:

TRACE A	WRITE
TRACE B	STORE VIEW
DGTL AVG	OFF
INPUT – B→A	OFF
SCALE	Full counterclockwise
INTEN	Midrange

4. Center FOCUS screwdriver adjustment on front panel.
5. Simultaneously press PLOT GRAT and LINE switch to turn instrument ON and display test routine #0. (Test routine number is displayed on left side of CRT.)

5-16. Z AXIS ADJUSTMENTS (Cont'd)

6. Press PLOT GRAT until test routine #3 is selected. (See Figure 5-4.) This routine displays, in CRT annotation, two rows of X's that are formed by a dot matrix. Press PLOT TRACE to vary the position of the two rows.

7. Set front-panel INTEN control fully clockwise. Adjust A3R30 ASTIG and A4R29 FOCUS LIMIT for sharpest dots at center of displayed annotation.

8. Decrease front-panel INTEN control until characters are dim but visible. Adjust A6R135 DYN FOCUS for sharpest dots displayed throughout displayed annotation.

9. Return front-panel INTEN control to midrange setting.

Pattern and Trace Align

10. Press PLOT GRAT to select test routine #4. Observe horizontal and vertical lines that trace perimeter of CRT display.

11. Adjust front panel TRACE ALIGN screwdriver adjustment to align both horizontal lines for best match to graticule perimeter.

12. Adjust A3R31 PATTERN potentiometer so that both horizontal and vertical traces have minimal curvature.

13. Repeat steps 6 through 12 **at least once** until no further adjustment is necessary.

Z Axis Frequency Response

14. Decrease display intensity with front-panel INTEN control until characters on CRT are dim but visible. Then adjust HF TRIM capacitor A6C61 and HF GAIN potentiometer A6R51 for the best uniformity of character intensity.

15. Set the front-panel INTEN control fully counterclockwise.

Minimum Intensity and Intensity Gain

16. Set controls as follows:

TRACE A	STORE BLANK
TRACE B	STORE BLANK
DGTL AVG	OFF
INP – B→A	OFF
SCALE	Full counterclockwise
INTEN	Full counterclockwise
FREQ SPAN/DIV	0 MHz
RESOLUTION BW	3 MHz
INPUT ATTEN	10 dB
REFERENCE LEVEL	–10 dBm
Amplitude Scale	LIN
SWEEP TRIGGER	FREE RUN
VIDEO FILTER	MAX (detent)

5-16. Z AXIS ADJUSTMENTS (Cont'd)

17. If spectrum analyzer plug-in is an HP 8559A, set SWEEP TIME/DIV to 2 μSEC and adjust A6R153 MIN INTEN potentiometer clockwise until trace disappears; then adjust counterclockwise until trace is barely visible.

    If spectrum analyzer plug-in is an HP 8558B or 8557A, set SWEEP TIME/DIV to 0.1 μSEC and adjust A6R153 MIN INTEN potentiometer clockwise until trace disappears; then adjust counterclockwise slightly past the point where the trace becomes visible.

18. Set SWEEP TIME/DIV to MAN. Turn MANUAL SWEEP control fully counterclockwise until dot is off screen.

19. Connect voltmeter to A6TP2 CONT GATE OUT. Gradually increase INTEN control to fully clockwise position. Voltage should not exceed +70V. Adjust A6R124 INTEN GAIN for a voltmeter reading of +70.0 ±0.2V.

NOTE

A16R153 MIN INTEN and A4R18 INT LIM affect the adjustment range of A6R124 INTEN GAIN. If A6R124 INTEN GAIN has insufficient adjustment range, repeat steps 15 – 19 to readjust A6R153 MIN INTEN. If A6R124 INTEN GAIN still lacks adequate adjustment range, perform High Voltage Power Supply Adjustment (paragraph 5-13) to adjust A4R18 INT LIM.

20. Disconnect voltmeter from A6TP2. Adjust INTEN and SCALE controls to midrange.

21. Set LINE switch off, disconnect power cord, and replace HP 853A top cover.

5-17. ANALOG DEFLECTION ADJUSTMENTS

REFERENCE:

A2 and A6 Schematics. See Figure 5-11 at the back of the section for locations of adjustments on assemblies A5 and A6.

DESCRIPTION:

With the HP 853A Display mainframe set for operation in the Analog Display mode, all digital circuitry is bypassed for a conventional analog display. The horizontal deflection circuitry is adjusted to ensure a centered 10-division CRT trace when a -5 to $+5$ volts horizontal sweep ramp is supplied by the spectrum analyzer plug-in. The vertical deflection circuitry is adjusted to ensure that video signals of 400, 800, and 0 millivolts place the CRT trace at the center, top, and bottom graticule lines respectively (i.e., a vertical deflection factor of 100 mV/division).

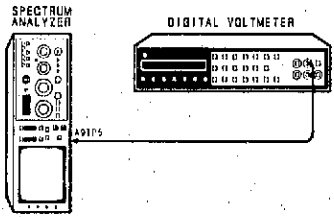


Figure 5-10. Analog Deflection Adjustments Test Setup

EQUIPMENT:

Digital Voltmeter	HP 3455A
Spectrum Analyzer plug-in	HP 8559A, 8558B, or 8557A

WARNING

To minimize shock hazard, use a non-metallic screwdriver for adjustments on XYZ Amplifier Assembly A6.

PROCEDURE:

1. Set LINE switch OFF, disconnect power cord and remove HP 853A top and bottom covers.

5-17. ANALOG DEFLECTION ADJUSTMENTS (Cont'd)

2. Reconnect power cord, set LINE switch ON, and connect equipment as shown in Figure 5-10. Set controls as follows:

TRACE A	STORE BLANK
TRACE B	STORE BLANK
DGTL AVG	OFF
INPUT – B→A	OFF
SCALE	Full counterclockwise
INTEN	Midrange
TUNING	>30 MHz
FREQ SPAN/DIV	0 MHz
RESOLUTION BW	3 MHz
INPUT ATTEN	10 dB
REFERENCE LEVEL	– 10 dBm
Amplitude Scale	LIN
SWEEP TIME/DIV	MAN
VIDEO FILTER	MAX (detent)

Horizontal Gain Adjustment

3. Adjust spectrum analyzer VERTICAL POSN screwdriver adjustment to position CRT dot approximately two divisions above bottom horizontal graticule line.

4. Adjust spectrum analyzer MANUAL SWEEP control for 0.00 ± 0.01 Vdc at A9TP5.

5. Adjust front-panel X POSN screwdriver adjustment to position CRT dot on center vertical graticule line.

NOTE

If the X POSN adjustment lacks adequate range or requires centering, change the values of factory-selected resistors A6R34* and A6R41* using Table 5-6.

Table 5-6. X POSN Factory-Selected Resistor Values

Desired Shift in Divisions	A6R34*	A6R41*
1 Right	10K	19.6K
½ Right	9.09K	16.2K
(Nominally Centered)	9.09K	17.8K
½ Left	9.09K	19.6K
1 Left	8.25K	19.6K

6. Adjust MANUAL SWEEP control for – 5.00 ± 0.01 Vdc at A9TP5.

7. Adjust A6R20 X GAIN potentiometer to position CRT dot on leftmost vertical graticule line.

5-17. ANALOG DEFLECTION ADJUSTMENTS (Cont'd)

NOTE

If A6R20 X GAIN lacks adequate adjustment range, change the value of factory-selected resistor A6R50*. Increase the value of the resistor if the gain is too high (CRT dot too far to the left); decrease the value of the resistor if the gain is too low.

8. Adjust MANUAL SWEEP control for +5.00 ±0.01 Vdc at A9TP5. CRT dot should be on rightmost vertical graticule line.

9. Repeat steps 4 – 8 until no further adjustment is necessary.

Vertical Gain Adjustment

10. Connect digital voltmeter to A9TP4. Adjust MANUAL SWEEP control to position CRT dot on center graticule line.

11. Adjust spectrum analyzer VERTICAL POSN screwdriver adjustment for a DVM reading of 0.00 ±0.01 Vdc at A9TP4.

12. Connect CAL OUTPUT signal to spectrum analyzer INPUT. Adjust REFERENCE LEVEL and TUNING controls to power level and frequency indicated on front panel next to CAL OUTPUT connector.

13. Adjust spectrum analyzer TUNING control for maximum voltage at A9TP4 (still tuned to CAL OUTPUT signal). Adjust REFERENCE LEVEL control for 0.40 ±0.01 Vdc at A9TP4.

14. Adjust front-panel Y POSN screwdriver adjustment to position CRT dot on center horizontal graticule line.

NOTE

If the Y POSN adjustment lacks adequate range or requires centering, change the values of factory-selected resistors A6R19* and A6R21* using Table 5-7.

Table 5-7. Y POSN Factory-Selected Resistor Values

Desired Shift in Divisions	A6R19*	A16R21*
1 Up	13.3K	9.09K
½ Up	16.2K	10K
(Nominally Centered)	17.8K	10K
½ Down	17.8K	9.09K
1 Down	16.2K	8.25K

5-17. ANALOG DEFLECTION ADJUSTMENTS (Cont'd)

15. Adjust spectrum analyzer TUNING for maximum voltage at A9TP4. Adjust REFERENCE LEVEL control for 0.80 ±0.01 Vdc at A9TP4.

16. Adjust A6R30 Y GAIN potentiometer to position CRT dot on topmost horizontal graticule line.

NOTE

If A6R30 Y GAIN lacks adequate adjustment range, change the value of factory-selected resistor A6R29*. Increase the value of the resistor if the gain is too high (CRT dot above topmost graticule line); decrease the value of the resistor if the gain is too low.

17. Disconnect CAL OUTPUT signal from spectrum analyzer INPUT and adjust VERTICAL POSN screwdriver adjustment for 0.00 ±0.01 Vdc at A9TP4. CRT dot should be on bottom horizontal graticule line.

18. Repeat steps 12 – 17 until no further adjustment is necessary.

19. When adjustment is complete, set LINE switch OFF, disconnect power cord, and install HP 853A top and bottom covers.

NOTE

To ensure that CRT plots made via HP-IB correspond to the CRT display, the digital storage adjustments (paragraph 5-15) should be performed after the analog deflection adjustments.

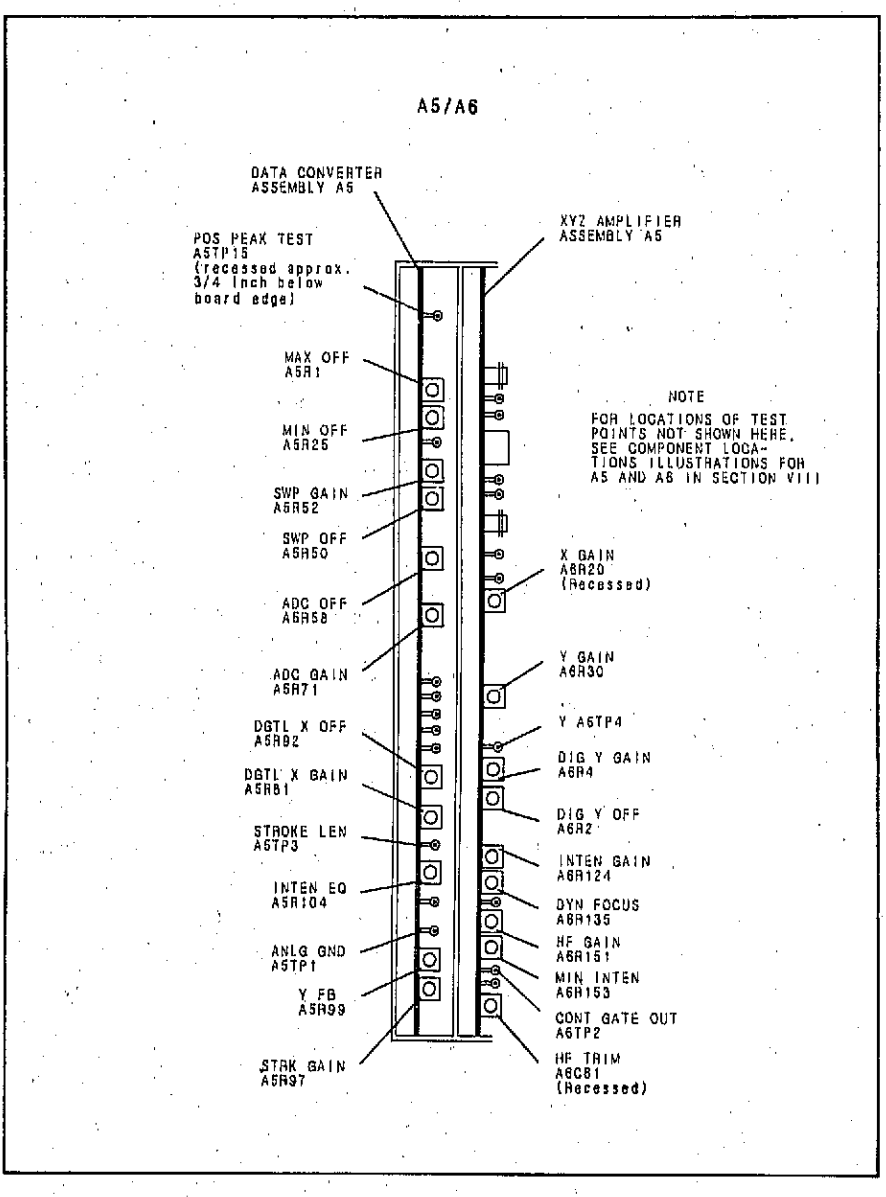


Figure 5-11. Data Converter Assembly A5 and XYZ Amplifier Assembly A6 Adjustments and Test Points Locations

PARTS LIST

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering replacement parts. Table 6-1 includes a list of reference designations and a list of abbreviations used in the parts list. Table 6-2 lists names and addresses that correspond to the manufacturer code numbers in the parts list. Table 6-3 lists all replaceable electrical parts in alpha-numerical order by reference designation. Table 6-3 also lists replaceable mechanical parts that are related to the board assemblies. All other replaceable mechanical parts are shown in Figures 6-1 through 6-7.

6-3. REPLACEABLE PARTS LIST

6-4. Table 6-3, the list of replaceable parts, is organized as follows:

1. Electrical assemblies and their components in alpha-numerical order by reference designation
2. Miscellaneous parts, with appropriate electrical assembly
3. Chassis-mounted electrical parts, in alpha-numerical order by reference designation
4. Mechanical chassis parts, at end of parts list

6-5. The following information is listed for each part:

1. The Hewlett-Packard part number
2. The part number check digit (CD)
3. The total quantity (Qty) in the instrument. This quantity is given only once, at the first appearance of the part in the list.
4. The description of the part
5. A five-digit code indicating a typical manufacturer of the part
6. The manufacturer's part number

6-6. ORDERING INFORMATION

6-7. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-8. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and number of parts required. Address the order to the nearest Hewlett-Packard office.

Table 6-1. Reference Designations and Abbreviations (1 of 3)

REFERENCE DESIGNATIONS

A ..... Assembly
AT ..... Attenuator, Isolator, Limiter, Termination
B ..... Fan, Motor
BT ..... Battery
C ..... Capacitor
CP ..... Coupler
CR ..... Diode, Diode Thyristor, Step Recovery Diode (SCR), Varactor
DC ..... Directional Coupler
DL ..... Delay Line
DS ..... Annunciator, Lamp, Light Emitting Diode (LED), Signalling Device (Audible or Visible)
E ..... Miscellaneous Electrical Part
F ..... Fuse
FL ..... Filter
H ..... Hardware
HY ..... Circulator
J ..... Electrical Connector (Stationary Portion), Jack
K ..... Relay
L ..... Coil, Inductor
M ..... Meter
MP ..... Miscellaneous Mechanical Part
P ..... Electrical Connector (Movable Portion), Plug
Q ..... Silicon Controlled Rectifier (SCR), Transistor, Triode Thyristor
R ..... Resistor
RT ..... Thermistor
S ..... Switch
T ..... Transformer
TB ..... Terminal Board
TC ..... Thermocouple
TP ..... Test Point
U ..... Integrated Circuit, Microcircuit
V ..... Electron Tube
VR ..... Breakdown Diode (Zener), Voltage Regulator
W ..... Cable, Transmission Path, Wire
X ..... Socket
Y ..... Crystal Unit (Piezoelectric, Quartz)
Z ..... Tuned Cavity, Tuned Circuit

ABBREVIATIONS

A

A ..... Across Flats, Acrylic, Air (Dry Method), Ampere
ADJ ..... Adjust, Adjustment
ANSI ..... American National Standards Institute (formerly USASI-ASA)
ASSY ..... Assembly
AWG ..... American Wire Gage

B

BCD ..... Binary Coded Decimal
BD ..... Board, Bundle
BE-CU ..... Beryllium Copper
BNC ..... Type of Connector
BR ..... Bearing, Boring
BRS ..... Brass
BSC ..... Basic
BTN ..... Button

C

C ..... Capacitance, Capacitor, Center Tapped, Centistoke, Cermet, Circular Mil Foot, Closed Cup, Cold, Compression
CCP ..... Carbon Composition Plastic
CD ..... Cadmium, Card, Cold-Drawn, Cord
CER ..... Ceramic
CHAM ..... Chamfer
CHAR ..... Character, Characteristic, Charcoal
CMOS ..... Complementary Metal Oxide Semiconductor
CNDCT ..... Conducting, Conductive, Conductivity, Conductor
CONT ..... Contact, Continuous, Control, Controller
CONV ..... Converter
CPRSN ..... Compression
CUP-PT ..... Cup Point
CW ..... Clockwise, Continuous Wave

D

D ..... Deep, Depletion, Depth, Diameter, Direct Current
DA ..... Darlington
DAP-GL ..... Diallyl Phthalate Glass
DBL ..... Double
DCDR ..... Decoder
DEG ..... Degree
D-HOLE ..... D-Shaped Hole
DIA ..... Diameter
DIP ..... Dual In-Line Package
DIP-SLDR ..... Dip Solder
D-MODE ..... Depletion Mode
DO ..... Package Type Designation
DP ..... Deep, Depth, Diametric Pitch, Dip
DPDTMINTR ..... Double Pole Three Throw, Miniature
DPDTMINFR .... Double Pole Double Throw, Miniature
DWL ..... Dowel

E

E-R ..... E-Ring
EXT ..... Extended, Extension, External, Extinguish

F

F ..... Fahrenheit, Farad, Female, Film (Resistor), Fixed, Flange, Flint, Fluorine, Frequency
FC ..... Carbon Film / Composition, Edge of Cutoff Frequency, Face
FDTHRU ..... Feed Through
FEM ..... Female
FIL-HD ..... Fillister Head
FL ..... Flush, Flat, Fluid
FLAT-PT ..... Flat Point
FR ..... Front
FREQ ..... Frequency
FT ..... Current Gain Bandwidth Product (Transition Frequency); Feet, Foot
FXD ..... Fixed

G

GEN ..... General, Generator
GND ..... Ground
GP ..... General Purpose, Group

H

H ..... Henry, Hermaphrodite, High, Hole Diameter, Hoi, Hub Inside Diameter, Hydrogen
HDW ..... Hardware
HEX ..... Hexadecimal, Hexagon, Hexagonal
HLCL ..... Helical
HP ..... Hewlett-Packard Company, High Pass, Horsepower

I

IC ..... Collector Current, Integrated Circuit
ID ..... Identification, Inside Diameter
IF ..... Forward Current, Intermediate Frequency
IN ..... Inch, Indium
INCL ..... Including
INT ..... Integral, Intensity, Internal
INTL ..... Internal, International

J

J-FET ..... Junction Field Effect Transistor
JFET ..... Junction Field Effect Transistor

K

K ..... Kelvin, Key, Kilo, Potassium
KNRLD ..... Knurled
KVDC ..... Kilovolts Direct Current

Table 6-1. Reference Designations and Abbreviations (2 of 3)

L

LED ..... Light Emitting Diode
LG ..... Length, Long
LIN ..... Linear, Linear Taper, Linearity
LK ..... Link, Lock
LKG ..... Leakage, Locking
LOGO ..... Logotype
LUM ..... Luminous

M

M ..... Male, Maximum, Mega, Mil, Milli, Mode, Momentary, Mounting Hole Centers, Mounting Hole Diameter
MA ..... Milliampere
MACH ..... Machined
MAX ..... Maximum
MC ..... Hot Molded Carbon Composition, Megacycle, Microcircuit, Molded Carbon Composition
MET ..... Metal, Metallic, Metallized, Metallurgical
MHZ ..... Megahertz
MIT ..... Miter
MLD ..... Mold, Molded
MM ..... Magnetized Material (Restricted Articles Code); Millimeter
MOM ..... Momentary
MTG ..... Mounting
MTLC ..... Metallic
MUW ..... Music Wire
MW ..... Milliwatt

N

N ..... Fan Out, Intrinsic Stand Off Ratio, Nano, Nanosecond, Nitrogen, None
N-CHAN ..... N-Channel
NH ..... Nanohenry
NM ..... Nanometer, Nunmetallic
NO ..... Normally Open, Number
NOM ..... Nominal
NPN ..... Negative Positive Negative (Transistor)
NS ... Nanosecond, Non-Shorting, Nose
NUM ..... Numeric, Numerical
NYL ..... Nylon (Polyamide)

O

OA ..... Other Restricted Articles, Group A (Restricted Articles Code); Over-All
OD ..... Olive Drab, Outside Diameter
OP AMP ..... Operational Amplifier
OPT ..... Optical, Option, Optional

P

PA ..... Picoampere, Power Amplifier, Pressure Angle, Praseodinium
PAN-HD ..... Pan Head
PAR ..... Parallel, Parity
PB ..... Lead (Metal), Push Button
PC ..... Picocoulomb, Piece, Printed Circuit
PCB ..... Printed Circuit Board
P-CHAN ..... P-Channel
PD ..... Pad, Palladium, Pitch Diameter, Power Dissipation
PF ..... Picofarad; Pipe, Female Connection; Power Factor
PKG ..... Package
PLSTC ..... Plastic
PNL ..... Panel
PNP ..... Positive Negative Positive (Transistor)
POLYC ..... Polycarbonate
POLYE ..... Polyester
POT ..... Potentiometer
POZI ..... Pozidriv Recess
PREC ..... Precision
PRP ..... Purple, Purpose
PSTN ..... Piston
PT ..... Part, Pint, Platinum, Point, Pulse Time
PW ... Power Wirewound, Pulse Width

Q

Q ..... Figure of Merit

R

R ..... Range, Red, Resistance, Resistor, Right, Ring, Rosin, Rubber-Resin, Run Torque
REF ..... Reference
RES .... Research, Resistance, Resistor
RF ..... Radio Frequency
RGD ..... Rigid
RND ..... Round
RR ..... Rear
RVT ..... Rivet, Riveted

S

SAWR ..... Surface Acoustic Wave Resonator
SEG ..... Segment
SGL ..... Single
SI ..... Silicon, Square Inch
SL ..... Slide, Slow
SLT ..... Slate, Slot, Slotted
SMA ..... Subminiature, A Type (Threaded Connector)
SMC ..... Subminiature, C Type (Threaded Connector)
SPCG ..... Spacing
SPDTSUBMIN .... Single Pole Double Throw, Subminiature
SPST .....Single Pole Single Throw
SQ ..... Square
SST ..... Stainless Steel
STL ..... Steel
SZ ..... Size

T

T ..... Tab Width, Taper, Teeth, Temperature, Tera, Tesla, Thermoplastic (Insulation), Thickness, Time, Timed, Tooth, Turns Ratio, Typical
TA ..... Ambient Temperature, Tantalum
TC ..... Thermoplastic
THD ..... Thread, Threaded
THK ..... Thick
TO ..... Package Type Designation, Troy Ounce
TPG ..... Tapping
TR-HD ..... Truss Head
TRMR ..... Trimmer
TRN ..... Turn, Turns
TRSN ..... Torsion

U

UCD ..... Microcandela
UF ..... Microfarad
UH ..... Microhenry
UL ..... Microliter, Underwriters' Laboratories, Inc.
UNHDND ..... Unhardened

V

V ..... Vanadium, Variable, Violet, Volt, Voltage
VAC ..... Vacuum; Volts, Alternating Current
VAC/DC ..... Volts, Alternating and Direct Current
VAR ..... Variable
VDC ..... Volts, Direct Current

W

W ..... Watt, Wattage, White, Wide, Width, Wire
W/CP ..... Wire / Conductive Plastic
W/SW ..... With Switch
WW ..... Wire Wound

X

X ..... By (Used With Dimensions), Reactance
XSTR ..... Transistor

Y

YIG ..... Yttrium-Iron-Garnet

Z

ZNR ..... Zener

Table 6-1. Reference Designations and Abbreviations (3 of 3)

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

Table 6-2. Manufacturers Code List

Mfr. No.	Manufacturer Name	Address	Zip Code
00000	ANY SATISFACTORY SUPPLIER		
00471	DOW-KEY CO INC	BROOMFIELD, WY	80020
01121	ALLEN-BRADLEY CO	MILWAUKEE, WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS, TX	75222
01542	HP DIV OI OPTOELECTRONICS	PALO ALTO, CA	94304
01613	GE CO SILICONE PRODUCTS BUS DEPT	WATERFORD, NY	12188
01808	SMALL PARTS INC	COSTA MESA, CA	92626
02111	SPECTROL ELECTRONICS CORP	CITY OF IND, CA	91745
02114	FERROXCUBE CORP	SAUGERTIES, NY	12477
02145	RAYCHEM CORP	MENLO PARK, CA	94025
02201	RICHCO PLASTIC INC	CHICAGO, IL	60646
02923	CHOMERICS INC	WOBURN, MA	01801
03480	HEYMAN MFG CO	KENTWORTH, NJ	07033
04225	THOMAS AND BETTS CO INC	ELIZABETH, NJ	
04480	BUSSMAN MFG DIV OF McGRAW-EDISON CO	EARTH CITY, MO	63178
04495	COMMERCIAL PLASTICS CO	MUNDELEIN, IL	60060
04604	FEDERAL SCREW PRODUCTS CO	CHICAGO, IL	60618
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	SANTA CLARA, CA	95050
04748	FEDERAL MOGUL CORP RBR AND PLASTIC GROUP	DETROIT, MICH	48235
04805	ILLINOIS TOOL WORKS INC SHAKEPROOF	ELGIN, IL	60120
04828	TINNERMAN PRODUCTS INC	CLEVELAND, OH	
05347	UNITED MINERAL AND CHEMICAL CORP	NEW YORK, NY	10013
06665	PRECISION MONOLITHICS INC	PHOENIX, AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW, CA	94042
08666	PANEL COMPONENTS CORPORATION	SANTA ROSA, CA	95401
17856	SILICONIX INC	SANTA CLARA, CA	95054
18324	SIGNETICS CORP	SUNNYVALE, CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS, TX	76067
24046	TRANSITRON ELECTRONIC CORP	WAKEFIELD, MA	01880
24355	ANALOG DEVICES INC	NORWOOD, MA	02062
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD, PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA, CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO, CA	94304
29832	TELEDYNE PHILBRICK NEXUS	DEDHAM, MA	02026
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE, NJ	
30161	AAVID ENGINEERING INC	LACONIA, NH	03246
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE, CA	94086
34649	INTEL CORP	MOUNTAIN VIEW, CA	95051
51642	CENTRE ENGINEERING INC	STATE COLLEGE, PA	16801
52063	EXAR INTEGRATED SYSTEMS INC	SUNNYVALE, CA	94086
52763	STETTNER-TRUSH INC	CAZENOVIA, NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS, MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE, SC	06226
75915	LITTELFUSE INC	DES PLAINES, IL	60016
84411	TRW CAPACITOR DIV	OGALLALA, NE	69153

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1A1	00853-60001	4	1	DISPLAY CONTROL ASSEMBLY	28480	00853-60001
A1A1DS1	1990-0487	7	8	LED-LAMP LUM-INT=1MCD IF=20MA-MAX RVR=5V	28480	1990-0487
A1A1J1	1251-6861	7	1	CONNECTOR 20-PIN M POST TYPE	28480	1251-6861
A1A1R1	2100-3631	5	2	RESISTOR-VAR CONTROL CP 10K 10% LIN	28480	2100-3631
A1A1R2	2100-3631	5		RESISTOR-VAR CONTROL CP 10K 10% LIN	28480	2100-3631
A1A1R4	0698-3445	2	2	RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-3480-F
A1A1S1	3101-2185	5	2	SWITCH-PB 4-STATION 10MM C-C SPACING	28480	3101-2185
A1A1S2	3101-2185	5		SWITCH-PB 4-STATION 10MM C-C SPACING	28480	3101-2185
A1A1S3	3101-2124	2	2	SWITCH-PB DPDT ALTNG .25A 115VAC	28480	3101-2124
A1A1S4	3101-2124	2		SWITCH-PB DPDT ALTNG .25A 115VAC	28480	3101-2124
A1A1S5	3101-2109	9	2	SWITCH-PB DPDT MOM .125A 115VAC	28480	3101-2109
A1A1S6	3101-2189	9		SWITCH-PB DPDT MOM .125A 115VAC	28480	3101-2109
A2	00853-60002	5	1	DISPLAY ADJUST ASSEMBLY	28480	00853-60002
A2E1	0360-1700	7	2	CONNECTOR-BCL CONT PIN .045-IN-BSC-BZ SO	28480	0360-1700
A2E2	0360-1700	7		CONNECTOR-BCL CONT PIN .045-IN-BSC-BZ SO	28480	0360-1700
A2MP1	0380-1512	7	1	STANDOFF- 9MM M3.0	28480	0380-1512
A2R1	2100-4007	1	1	RESISTOR-VAR 1 MEGOHM 10% 17	28480	2100-4007
A2R2	2100-4010	6	2	RESISTOR-VAR 5K OHM 10% 17	28480	2100-4010
A2R3	2100-4009	3	1	RESISTOR-VAR 2.5 K 10% 17	28480	2100-4009
A2R4	2100-4010	6		RESISTOR-VAR 5K OHM 10% 17	28480	2100-4010
A3	00853-60003	6	1	DISPLAY POWER SUPPLY ASSEMBLY	28480	00853-60003
A3C1	0160-3456	8		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A3C2	0160-3454	4	1	CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3454
A3C3	0180-0114	1	21	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A3C4	0180-0291	3	26	CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A3C5	0160-4004	8	17	CAPACITOR-FXD .10F +-20% 50VDC CER	28480	0160-4004
A3C6	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A3C7	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A3C8	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A3C9	0160-4004	8		CAPACITOR-FXD .10F +-20% 50VDC CER	28480	0160-4004
A3C10	0160-4004	8		CAPACITOR-FXD .10F +-20% 50VDC CER	28480	0160-4004
A3C11	0180-0291	3		CAPACITOR-FXD 10F +-10% 35VDC TA	56289	150D106X9035A2
A3C12	0180-0412	8	1	CAPACITOR-FXD 0.068UF+75-10% 330VDC AL	28480	0180-0412
A3C13	0160-5214	8		CAPACITOR-FXD .01F +-20% 500VDC CER	28480	0160-5214
A3C14	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A3C15	0160-4002	8	5	CAPACITOR-FXD .02UF +-10% 100VDC CER	28480	0160-4002
A3C16	0160-5100	9	8	CAPACITOR-FXD .01UF +-10% 1000VDC CER	28480	0160-5100
A3C17	0160-5100	9		CAPACITOR-FXD .01UF +-10% 1000VDC CER	28480	0160-5100
A3C18	0160-4004	8		CAPACITOR-FXD .10F +-20% 50VDC CER	28480	0160-4004
A3C19	0160-4004	8		CAPACITOR-FXD .10F +-20% 50VDC CER	28480	0160-4004
A3CR1	1901-0050	3	37	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR2	1901-0743	1	28	DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR3	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR4	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR5	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR6	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR8	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR9	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR10	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR11	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR12	1901-0662	3	4	DIODE-PWR RECT 100V 6A	04713	MR751
A3CR13	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A3CR14	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A3CR15	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A3CR16	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR17	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR18	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR20	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A3CR21	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3DS1	1990-0407	7		LED-LAMP LUM-INT=1MCD IF=20MA-MAX VR=5V	28480	5082-4504
A3DS2	1990-0407	7		LED-LAMP LUM-INT=1MCD IF=20MA-MAX VR=5V	28480	5082-4504
A3DS3	1990-0407	7		LED-LAMP LUM-INT=1MCD IF=20MA-MAX VR=5V	28480	5082-4504
A3DS4	1990-0407	7		LED-LAMP LUM-INT=1MCD IF=20MA-MAX VR=5V	28480	5082-4504
A1F1	2110-0610	3	1	FUSE 5A 125V NTD .25X.97	28480	2110-0610
A2F2	2110-0333	9	4	FUSE 1.5A 125V .25X.27	28480	2110-0333
A1F3	2110-0333	9		FUSE 1.5A 125V .25X.27	28480	2110-0333
A3F4	2110-0343	1	1	FUSE .25A 125V NTD .091X.093	28480	2110-0343
A1J1	1251-3083	3	1	CONNECTOR 8-PIN M POST TYPE	28480	1251-3083
A3J2	1251-7564	9	1	CONNECTOR-HEADER 14 M 1R	28480	1251-7564
A3J3	1251-7557	0	1	CONNECTOR-HEADER 4 M 1R	28480	1251-7557
A3MP1	1251-2313	6	10	CONNECTOR-SGL CONT SKT .04-IN-BOC-02 RND	28480	1251-2313
A3MP2	1205-0043	8	4	INSULATOR-XSTR ALUMINUM	28480	1205-0043
A3MP3	0515-0211	8	8	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A3MP4	3050-0891	7	13	WASHER-FL MTLC 3.0 MM 3.5 MM-ID	28480	3050-0891
A3MP5	0340-0867	9	3	INSULATOR-FLG-DBHC NYLON	28480	0340-0867
A3MP6	0340-0864	6	3	INSULATOR-XSTR THRM-CNDCT	28480	0340-0864
A3MP7	0515-0417	4	3	SCREW-MACH M3 X 0.5 10MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A3MP8	2190-0005	0	8	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
A3MP9	0515-0105	9	8	SCREW-MACH M3 X 0.5 12MM-LG PAN-HD	28480	0515-0105
A3MP10	0535-0004	9	12	NUT-HEX DBL-CHAM M3 X 0.5 2.4MM-THK	00000	ORDER BY DESCRIPTION
A3MP11	0340-0140	1	1	INSULATOR-XSTR MICA	28480	0340 140
A3MP12	0380-3240	8	4	STANDOFF-RVT-DN 14-MM-LG 6.17-MM-OD BRS	00000	ORDER BY DESCRIPTION
A3MP13	2680-0129	0	0	SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A3MP14	00853-20030	5	1	HEAT SINK-DISPLAY POWER	28480	00853-20030
A3MP15	2190-0011	0	0	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
A1Q1	1854-0311	0	2	TRANSISTOR NPN 2N4240 DI TO-66 PD=35W	04713	2N4240
A1Q2	1854-0232	2	7	TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0232
A1Q3	1853-0021	7	1	TRANSISTOR PNP 2N5416 SI TO-5 PD=1W	04713	2N5416
A1Q4	1854-0232	2		TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0232
A1Q5	1854-0232	2		TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0232
A3Q6	1884-0011	4	2	THYRISTOR-SCR 2N4005 TO-220AB VRRM=100	04713	2N4005
A3Q7	1884-0073	2	2	THYRISTOR-SCR TO-5 VRRM=100	28480	1884-0073
A3Q8	1884-0073	2		THYRISTOR-SCR TO-5 VRRM=100	28480	1884-0073
A1R1	0757-0279	0	9	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A1R2	0683-1105	5	3	RESISTOR 1M 5% .25W FC TC=-400/+600	01121	EB1055
A1R3	0698-3260	9	2	RESISTOR 464K 1% .125W F TC=0+-100	28480	0698-3260
A1R4	0698-3455	4	1	RESISTOR 261K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2613-F
A1R7	0698-3153	9	1	RESISTOR 3.03K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3031-F
A1R8	0757-0854	7	1	RESISTOR 56.2K 1% .5W F TC=0+-100	28480	0757-0854
A1R9	0757-0855	8	1	RESISTOR 60.4K 1% .5W F TC=0+-100	28480	0757-0855
A1R10	0698-3439	4	3	RESISTOR 170 1% .125W F TC=0+-100	24546	C4-1/8-T0-1700-F
A1R12	0757-0279	9	7	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A1R13	0757-0445	4	4	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-1620-F
A1R13	0757-0279	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A1R14	0698-3439	4		RESISTOR 170 1% .125W F TC=0+-100	24546	C4-1/8-T0-1700-F
A1R15	0757-0445	4		RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-1620-F
A1R16	0698-3447	4	0	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-4220-F
A1R17	0698-3132	4	6	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A1R18	0757-0401	0	23	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R19	0757-0346	2	14	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1R20	2100-1771	0	4	RESISTOR-TRMR 200 5% 1W TOP-ADJ 1-TRN	28480	2100-1771
A1R21	2100-1771	0		RESISTOR-TRMR 200 5% 1W TOP-ADJ 1-TRN	28480	2100-1771
A1R22	0757-0279	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A1R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R24	0698-8030	9	1	RESISTOR 5.9K .05% .125W F TC=0+-50	19701	MFA1/8-T9-5901-C
A1R25	0757-0279	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A1R26	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R27	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A3R28	2100-1770	9	1	RESISTOR-TRMR 100 5% 1W TOP-ADJ 1-TRN	28480	2100-1770
A3R29	0757-0462	3	2	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A3R30	2100-0580	7	2	RESISTOR-TRMR 500K 10% C TOP-ADJ 1-TRN	28480	2100-0580
A3R31	2100-0580	7		RESISTOR-TRMR 500K 10% C TOP-ADJ 1-TRN	28480	2100-0580
A3R32	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-4220-F
A1R33	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-4220-F
A3R34	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-4220-F
A3R35	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-4220-F
A3TP1	0360-0535	8	A5	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP2	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP3	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP4	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP5	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP6	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP7	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U1	1826-0393	7	1	IC V REGLTR TO-220	27014	LM317
A3U2	1826-0221	0	1	IC V REGLTR TO-220	04713	MC7912CT
A3U3	1826-0317	9	1	IC 337 V REGLTR TO-220	27014	LM337T
A3U4	1826-0631	6	2	IC-ANOM HYBRID	28480	1826-0631
A3VR1	1902-3059	A	2	DIODE-ZNR 7.03V 5% DO-35 PD=.4W	28480	1902-3059
A3VR2	1902-0793	3	3	DIODE-ZNR 1N944 10.7V 5% DO-7 PD=.5W	04713	1N944
A3VR3	1902-0793	3		DIODE-ZNR 1N944 10.7V 5% DO-7 PD=.5W	04713	1N944
A3VR4	1902-0049	2	4	DIODE-ZNR 6.19V 5% DO-35 PD=.4W	28480	1902-0049
A3VR5	1902-0660	1	2	DIODE-ZNR 200V 5% DO-35 PD=1W TC=+.060%	28480	1902-0660
A3VR6	1902-3402	7	1	DIODE-ZNR 68.6V 2% DO-7 PD=.4W TC=+.001%	28480	1902-3402
A3VR7	1902-3223	8	2	DIODE-ZNR 12.4V 2% DO-35 PD=.4W	28480	1902-3223
A3VR8	1902-3233	0		DIODE-ZNR 12.4V 2% DO-35 PD=.4W	28480	1902-3233
A4	08569-60005	9	1	HIGH-VOLTAGE POWER SUPPLY ASSEMBLY	28480	08569-60005
A4A1	08569-60008	0	1	TRANSFORMER-HIGH VOLTAGE	28480	08569-60008
A4C1	0180-0141	2	3	CAPACITOR-FXD 560UF+75-10% 50VDC AL	56289	30D506G050DD2
A4C2	0180-0141	2		CAPACITOR-FXD 560UF+75-10% 50VDC AL	56289	30D506G050DD2
A4C3	0180-0141	2		CAPACITOR-FXD 560UF+75-10% 50VDC AL	56289	30D506G050DD2
A4C4	0160-3665	9	2	CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A4C5	0160-4297	5	2	CAPACITOR-FXD .022UF +80-20% 1000VDC CER	56289	C0F3F1B1H223Z5P2-CDH
A4C6	0160-4297	5		CAPACITOR-FXD .022UF +80-20% 1000VDC CER	56289	C0F3F1B1H223Z5P2-CDH
A4C7	0160-4004	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4004
A4C8	0170-0048	9	1	CAPACITOR-FXD .047UF +-10% 200VDC POLYE	56289	292P47392
A4C9	0160-4051	9	4	CAPACITOR-FXD .01UF +-20% 4KVDC	28480	0160-4051
A4C10	0160-4051	9		CAPACITOR-FXD .01UF +-20% 4KVDC	28480	0160-4051
A4C11	0160-0162	5	1	CAPACITOR-FXD .022UF + 10% 200VDC POLYE	28480	0160-0162
A4C12	0160-0614	6	4	CAPACITOR-FXD 1000PF +-20% 4KVDC	28480	0160-0614
A4C13	0109-0249	5	2	CAPACITOR-FXD 1UF +50-10% 150VDC AL	56289	30D105G150DA2
A4C14	0160-0614	6		CAPACITOR-FXD 1000PF +-20% 4KVDC	28480	0160-0614
A4C15	0160-4051	9		CAPACITOR-FXD .01UF +-20% 4KVDC	28480	0160-4051
A4C16	0180-0149	5		CAPACITOR-FXD 10UF+50-10% 150VDC AL	56289	30D106G150DA2
A4C17	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A4C18	0160-0614	6		CAPACITOR-FXD 1000PF +-20% 4KVDC	28480	0160-0614
A4C19	0160-0614	6		CAPACITOR-FXD 1000PF +-20% 4KVDC	28480	0160-0614
A4C20	0160-4051	9		CAPACITOR-FXD .01UF +-20% 4KVDC	28480	0160-4051
A4CR1	1901-0050	3		DIODE-SWITCHING 40V 200MA 2NS DO-35	28480	1901-0050
A4CR2	1901-0050	3		DIODE-SWITCHING 40V 200MA 2NS DO-35	28480	1901-0050
A4CR3	1901-0028	5	24	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR4	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR5	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR6	1901-0050	3		DIODE-SWITCHING 40V 200MA 2NS DO-35	28480	1901-0050
A4CR7	1901-0050	3		DIODE-SWITCHING 40V 200MA 2NS DO-35	28480	1901-0050
A4CR8	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR9	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR10	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR11	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR12	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR13	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR14	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4CR15	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A4F1	2110-0891	0	1	FUSE 1A 250V NTD 1.25X.25 UL	75915	312001
A4J1				NOT ASSIGNED		
A4J2	1251-4602	6	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-4602
A4J3	1251-4316	3	1	CONNECTOR 7-PIN M POST TYPE	28480	1251-4316
A4L1	9140-0171	3	2	INDUCTOR RF-CH MLD 400UH 10% .12VADX.96DCR	28480	9140-0171
A4L2	9140-0171	3		INDUCTOR RF-CH MLD 400UH 10% .12VADX.96DCR	28480	9140-0171
A4L3	9140-0129	1	1	INDUCTOR RF-CH MLD 220UH 5% .16ADX.805CR	28480	9140-0129
A4MP1	1400-0073	6	6	PIN-KOLL .062-IN-DIA .25-IN-LG BE-CU	28480	1400-0073
A4MP2	2110-0049	8	2	FUSEHOLDER-CLIP TYPE.250-FUSE	28480	2110-0049
A4MP3	2200-0111	2	2	SCREW-MACH 4-40 .5-IN-LG PAN HD-POZI	00000	ORDER BY DESCRIPTION
A4MP4	2200-0099	3	2	NUT-HEX-W/LKWR 4-40 THD .094 IN-THK	00000	ORDER BY DESCRIPTION
A4MP5	2200-0099	4	1	SCREW-MACH 6-32 1.25-IN LG PAN HD-SLT	00000	ORDER BY DESCRIPTION
A4MP6	2580-0012	6	1	NUT-HEX-DBL-CHAM 6-32 THD .125-IN-THK	00000	ORDER BY DESCRIPTION
A4MP7	4040-0754	1	2	EXTR-PC BD MLD POLYC .062-DD-THKNS	28480	4040-0754
A4MP8	4040-0454	8		THERMAL COMPOUND	28480	4040-0454
A4MP9	08569-60010	0	1	COVER-HIGH VOLTAGE	28480	08569-60010
A4MP10	08569-60006	4	1	HEAT SINK-HIGH-VOLTAGE	28480	08569-60006
A4MP11	1200-0843	0		INSULATOR-XSTR ALUMINUM	28480	1200-0843
A4MP12	1200-0811	4	2	INSULATOR-FLG-DIOD NYLON	28480	1200-0811
A4MP13	1200-0174	5	12	INSULATOR-XSTR DAP-GL	28480	1200-0174
A4MP14	1205-0605	0	12	HEAT SINK-TO TO-5/TO-39 EO	33161	52259
A4MP15	1251-0600	0	5	CONNECTOR-RFI PCMT PIN 1.14-OD DCC-07 BO	28480	1251-0600
A4Q1	1854-0510	7	1	TRANSISTOR NPN 2N5027 ST TO-3 PD=180W	04713	2N5027
A4Q2	1854-0404	0	28	TRANSISTOR NPN ST TO-18 PD=360MW	28480	1854-0404
A4Q3	1854-0361	0	1	TRANSISTOR NPN 2N4239 ST TO 5 PD=6W	04713	2N4239

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R1	0757-0279	8		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A4R2	BA98-0884	9	13	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R3	0757-0339	3	1	RESISTOR 511K 1% .5W F TC=0+-100	28480	0757-0339
A4R4	0100-3061	5	1	RESISTOR-TRMR 500K 10% C 0100-ADJ 17-TRN	02111	43P504
A4R5	0757-0465	6	14	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R6	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R7	0683-2265	8	1	RESISTOR 22M 5% .25W FC TC=-900/+1200	01121	CB2265
A4R8	0757-0401	8		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R9	0698-3162	0	3	RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A4R10	0698-3484	3	1	RESISTOR 383 1% .5W F TC=0+-100	28480	0698-3484
A4R11	0757-0280	3	16	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R12	0698-0737	5	1	RESISTOR 103K 5% .25W CC TC=-400/+800	28480	0698-0737
A4R13	0699-0751	9	1	RESISTOR 5.4K 5% .25W CC TC=-400/+700	28480	0699-0751
A4R14	0699-0167	1	1	RESISTOR 30M 5% 1W C TC=0+-250	28480	0699-0167
A4R15	0687-3941	8	2	RESISTOR 390M 10% .5W FC TC=0+0D2	01121	EB3941
A4R16	0699-0743	9	8	RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R17	0698-3159	8	1	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A4R18	2100-3054	6	1	RESISTOR-TRMR 50K 10% C 0100-ADJ 17-TRN	02111	43P503
A4R19	0699-0743	9		RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R20	0699-0743	9		RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R21	0683-1065	7	2	RESISTOR 10M 5% .25W CC TC=-900/+1100	01121	CB1065
A4R22	0699-0743	9		RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R23	0698-0748	2	1	RESISTOR 100 5% .25W CC TC=-400/+500	28480	0698-0748
A4R24	0683-1005	5		RESISTOR 10 5% .25W FC TC=-400/+300	01121	CB1005
A4R25	0687-3941	8		RESISTOR 390M 10% .5W FC TC=0+0D2	01121	EB3941
A4R26	0699-0743	9		RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R27	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R28	0699-0177	8	1	RESISTOR 3M 5% 1W C TC=0+-250	28480	0699-0177
A4R29	2100-3358	3	1	RESISTOR-TRMR 1M 20% C 0100-ADJ-1-TRN	28480	2100-3358
A4R30	0699-0551	7	1	RESISTOR 5.3M 5% 1W C TC=0+-250	28480	0699-0551
A4R31	0699-0743	9		RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R32	0699-0743	9		RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R33	0683-1065	7		RESISTOR 10M 5% .25W CC TC=-900/+1100	01121	CB1065
A4R34	0699-0743	9		RESISTOR 600 5% .25W CC TC=-400/+600	28480	0699-0743
A4R35	0683-1035	5		RESISTOR 10 5% .25W FC TC=-400/+500	01121	CB1035
A4TP1				NOT ASSIGNED		
A4TP2	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP3	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP4	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP5	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP6	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4U1				NOT ASSIGNED		
A4U2	1826-0167	3	1	IC OP AMP PRGMBL TO-99 PKG	27095	CA3094AT
A4VR1	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A4VR2	1902-3393	05	1	DIODE-ZNR 75V 5% DO-7 PD=.4W TC=4.077%	28480	1902-3393
A4VR3	2140-0018	0	2	LAMP-GLOW NEON-GT 90VDC 250UA T-3-DUAL	08473	NEON-GT
A4VR4	2140-0018	0		LAMP-GLOW NEON-GT 90VDC 250UA T-3-DUAL	08473	NEON-GT
A4VR5	1902-3394	4	1	DIODE-ZNR 750 2% DO-7 PD=.4W TC=+.322%	28480	1902-3394
A4VR6	1902-0125	05	1	DIODE-ZNR 100V 5% PD=1W IR=5UA	28480	1902-0125
A4VR7	1902-0460	1		DIODE-ZNR 200V 5% DO-15 PD=1W TC=+.380%	28480	1902-0460
A4VR8	1902-0197	1	1	DIODE-ZNR 82V 5% PD=1W IR=5UA	28480	1902-0197
A5	00853-60007	0	1	DATA CONVERTER ASSEMBLY	28480	00853-60007
A5C1	0160-3079	7	A1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C2	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C3	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C4	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C5	0160-0745	2	3	CAPACITOR-FXD 910PF +-5% 100VDC MICA	28480	0160-0745
A5C6	0160-3077	5	4	CAPACITOR-FXD 130PF +-20% 200VDC CER	28480	0160-3077
A5C7	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C8	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C9	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C10	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C11	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C12	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C13	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C14	0160-0745	2		CAPACITOR-FXD 910PF +-5% 100VDC MICA	28480	0160-0745
A5C15	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C16	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C17	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C18	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C19	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A5C20	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079

See Introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr. Code	Mfr Part Number
A5C31	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C32	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C33	0180-0197	8	P	CAPACITOR-FXD 3.3UF+-10% 20VDC TA	56289	150D335X9020B2
A5C34	0160-3879	7		CAPACITOR-FXD .01UF + 20% 100VDC CER	28480	0160-3879
A5C35	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C36	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C37	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C38	0160-0943	2		CAPACITOR-FXD 910PF +-5% 100VDC MICA	28480	0160-0943
A5C39	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C40	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C41	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C42	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C43	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C44	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C45	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C46	0160-3878	6	2	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C47	0160-3533	8	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	28480	0160-3533
A5C48	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C49	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C50	0160-4624	2	1	CAPACITOR-FXD 0.020PF +-.5% 500VDC CER	28480	0160-4624
A5C51	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A5C52	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C53	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C54	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C55	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C56	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C57	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C58	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C59	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C60	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C61	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C62	0180-0291	3		CAPACITOR-FXD 10F +-10% 35VDC TA	56289	150D106X9035A2
A5C63	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C64	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C65	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C66	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C67	0160-4498	8	P	CAPACITOR-FXD 5.6PF +-.5PF 500VDC CER	28480	0160-4498
A5C68	0160-0571	3	1	CAPACITOR-FXD 0.47UF +-20% 100VDC CER	28480	0160-0571
A5C69	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C70	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C71	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C72	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C73	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C74	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C75	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C76	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C77	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C78	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C79	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C80	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C81	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035A2
A5C82	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C83	0160-4498	8		CAPACITOR-FXD 5.6PF +-.5PF 500VDC CER	28480	0160-4498
A5C85	0160-3875	3	1	CAPACITOR-FXD 220F +-5% 300VDC CER 0+-30	28480	0160-3875
A5C86	0180-0197	8		CAPACITOR-FXD 3.3UF+-10% 20VDC TA	56289	150D335X9020B2
A5CR1	1901-0539	3	7	DIODE-GP SIG SCHOTTKY	28480	1901-0539
A5CR2	1901-0376	6	3	DIODE-GEN PUP 35V 50MA DO-35	28480	1901-0376
A5CR3	1901-0539	3		DIODE-GP SIG SCHOTTKY	28480	1901-0539
A5CR4	1901-0376	6		DIODE-GEN PUP 35V 50MA DO-35	28480	1901-0376
A5CR5	1901-0539	3		DIODE-GP SIG SCHOTTKY	28480	1901-0539
A5CR6	1901-0539	3		DIODE-GP SIG SCHOTTKY	28480	1901-0539
A5CR7	1901-0539	3		DIODE-GP SIG SCHOTTKY	28480	1901-0539
A5CR8	1901-0058	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR9	1901-0058	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR10	1901-0539	3		DIODE-GP SIG SCHOTTKY	28480	1901-0539

See introduction to this section for ordering information
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR13	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A5CR14	1901-0033	2	1	DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A5CR15	1901-1080	5	1	DIODE-SM SIG SCHOTTKY	28480	1901-1080
A5L1	9140-0210	1	17	INDUCTOR RF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A5L2	9140-0210	1		INDUCTOR RF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A5L3	9140-0210	1		INDUCTOR RF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A5L4	9140-0210	1		INDUCTOR RF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A5L5	9100-1788	6	2	CHOKE-WIDE BAND ZMAX=680 OHM@ 180 MHZ	02114	VK200 20/4B
A5L6	9140-0210	1		INDUCTOR RF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A5L7	9100-1627	2	1	INDUCTOR RF-CH-MLD 39UH 5% .166DX.385LG	28480	9100-1627
A5L8	9140-0210	1		INDUCTOR RF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A5L9	9140-0210	1		INDUCTOR RF-CH-MLD 100UH 5% .166DX.385LG	28480	9140-0210
A5MP1	0380-1513	0	2	STANDOFF-SHML M3.0	28480	0380-1513
A5MP2	4040-0747	2	2	EXTR-PC BD GRA POLYC .062-BD-THKNS	28480	4040-0747
A5MP3	1480-0073	6		PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU	28480	1480-0073
A5Q1	1855-0241	5	6	TRANSISTOR MOSFET N-CHAN E-MODE TO-72 SI	18324	SD215
A5Q2	1855-0241	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-72 SI	18324	SD215
A5Q3	1855-0241	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-72 SI	18324	SD215
A5Q4	1855-0241	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-72 SI	18324	SD215
A5Q5	1853-0034	0	3	TRANSISTOR PNP SI TO-18 PD=360MW	28480	1853-0034
A5Q6	1853-0034	0		TRANSISTOR PNP SI TO-18 PD=360MW	28480	1853-0034
A5Q7	1854-0404	0		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A5Q8	1855-0241	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-72 SI	18324	SD215
A5Q9	1854-0404	0		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A5Q10	1855-0050	4	3	TRANSISTOR-JFET DUAL N-CHAN D-MODE SI	28480	1855-0050
A5Q11	1854-0475	5	5	TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0475
A5Q12	1853-0316	1	2	TRANSISTOR-DUAL PNP PD=530MW	28480	1853-0316
A5Q13	1853-0302	9	1	TRANSISTOR PNP 2N2946A SI TO-46 PD=400MW	01295	2N2946A
A5Q14	1853-0034	0		TRANSISTOR PNP SI TO-18 PD=360MW	28480	1853-0034
A5Q15	1855-0050	4		TRANSISTOR-JFET DUAL N-CHAN D-MODE SI	28480	1855-0050
A5Q16	1853-0075	9	2	TRANSISTOR-DUAL PNP PD=400MW	28480	1853-0075
A5Q17	1854-0475	5		TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0475
A5Q18	1854-0404	0		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A5Q19	1855-0241	5		TRANSISTOR MOSFET N-CHAN E-MODE TO-72 SI	18324	SD215
A5Q20	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
A5Q21	1855-0050	4		TRANSISTOR-JFET DUAL N-CHAN D-MODE SI	28480	1855-0050
A5Q22	1855-0420	2	2	TRANSISTOR J-FET 2N4391 N-CHAN D-MODE	01295	2N4391
A5Q23	1855-0420	2		TRANSISTOR J-FET 2N4391 N-CHAN D-MODE	01295	2N4391
A5Q24	1854-0475	5		TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0475
A5Q25	1853-0075	9		TRANSISTOR-DUAL PNP PD=400MW	28480	1853-0075
A5Q26	1854-0475	5		TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0475
A5R1	2100-3353	8	4	RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	28480	2100-3353
A5R2	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R3	0698-3132	4		RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A5R4	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R5	0757-0438	3	15	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R6	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R8	0757-0274	5	4	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
A5R9	0698-3440	7	2	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A5R10	0698-0083	8	7	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A5R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A5R12	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R13	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A5R14	0698-3150	6	4	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A5R15	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R16	0757-0199	3	2	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A5R17	0698-3152	8	4	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A5R18	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A5R19	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A5R20	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R21	0698-3132	4		RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A5R22	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A5R23	0698-3151	7	5	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A5R24	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A5R25	2100-3353	8		RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	28480	2100-3353
A5R26	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R29	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R30	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R31	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R32	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
A5R33	0757-0416	7	5	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R34	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R36	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A5R37	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A5R38	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A5R39	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A5R40	0698-3132	4		RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A5R41	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R42	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R43	0698-3132	4		RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A5R44	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A5R45	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R46	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A5R47	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R48	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A5R49	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A5R50	2100-3273	1	4	RESISTOR-TRMR 2K 10% C SIDE-ADJ 1-TRN	28480	2100-3273
A5R51	0698-3155	1	4	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A5R52	2100-3350	5	4	RESISTOR-TRMR 200 10% C SIDE-ADJ 1-TRN	28480	2100-3350
A5R53	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A5R54	0698-3154	0	1	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A5R55	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R56	0757-0440	7	5	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A5R57	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A5R58	2100-3353	8		RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	28480	2100-3353
A5R59	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5R60	0757-1094	9	6	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A5R61	0757-0289	2	4	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A5R62	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R63	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A5R64	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R65	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A5R66	0698-3152	8		RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A5R67	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A5R68	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A5R69	0757-0288	1		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A5R70	0757-0422	5	2	RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A5R71	2100-3350	5		RESISTOR-TRMR 200 10% C SIDE-ADJ 1-TRN	28480	2100-3350
A5R72	0698-3132	4		RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A5R72	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R73	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R74	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A5R75	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R76	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R77	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R78	0757-0444	1	2	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A5R79	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R80	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R81	2100-3273	1		RESISTOR-TRMR 2K 10% C SIDE-ADJ 1-TRN	28480	2100-3273
A5R82	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A5R83	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R84	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R85	0698-7878	3	1	RESISTOR 150K 1% .125W F TC=0+-25	19701	MF4C1/8-T9-1503-F
A5R86	0757-0462	3		RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A5R87	0757-0476	9	1	RESISTOR 301K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3013-F
A5R88	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R89	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R90	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A5R91	0757-0289	2		RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A5R92	2100-3350	5		RESISTOR-TRMR 200 10% C SIDE-ADJ 1-TRN	28480	2100-3350
A5R93	0757-0422	5		RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A5R94	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A5R95	0757-0420	3	3	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A5R96	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A5R97	2100-3273	1		RESISTOR-TRMR 2K 10% C SIDE-ADJ 1-TRN	28480	2100-3273
A5R98	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A5R99	2100-3350	5		RESISTOR-TRMR 200 10% C SIDE-ADJ 1-TRN	28480	2100-3350
A5R100	0757-0418	9	2	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A5R101	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R102	0698-3136	8		RESISTOR 17.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1782-F
A5R103	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A5R104	2100-3352	7	3	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A5R105	0698-6347	9	1	RESISTOR 1.5K .1% .125W F TC=0+-25	28480	0698-6347
A5R106	0698-6624	5	4	RESISTOR 2K .1% .125W F TC=0+-25	28480	0698-6624
A5R107	0698-6624	5		RESISTOR 2K .1% .125W F TC=0+-25	28480	0698-6624

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R108	0698-6624	5		RESISTOR 2K .1% .125W F TC=0+-25	28480	0698-6624
A5R109	0698-6624	5		RESISTOR 2K .1% .125W F TC=0+-25	28480	0698-6624
A5R116	0757-0444	1		RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A5R117	0698-3445	2		RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
A5R118	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A5R119	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A5R120	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A5R121	0698-3457	6	2	RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A5R122	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A5R123	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R124	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A5TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP13	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP14	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP15	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5U1	1826-0462	1	1	IC CONV 18-B-D/A 16-DIP-C PKG	04713	MC3410CL
A5U2	1826-0371	1	1	IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	27014	LF256H
A5U3	1826-0703	9	1	IC OP AMP LOW-NOISE 8-DIP-C PKG	52063	XR5534ACN
A5U4	1826-0092	3	1	IC OP AMP GP DUAL TO-99 PKG	28480	1826-0092
A5U5	1820-2052	4	1	IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
A5U6	1826-1904	2	1	IC CONV 10-B-D/A 16-DIP-C PKG	24355	AD561KD
A5U7	1826-0026	3	3	IC COMPARATOR PRCN TO-99 PKG	01295	LM311L
A5U8	1820-1978	4	1	IC RGTR TTL L 12-BIT	34335	AM25L04PC
A5U9	1826-0082	8	1	IC OP AMP WB TO-99 PKG	29032	1322
A5U10	1820-1546	2	1	IC MULTIPLXR 4-CHAN-ANLG DUAL 16-DIP-C	04713	MC14052BCL
A5U11	1826-0458	5	2	IC OP AMP TO-99 PKG	27014	LF255H
A5U12	1826-0705	1	2	IC OP AMP LOW-BIAS-H-IMPD DUAL 8-DIP-C	01295	TL072ACJG
A5U13	1826-0026	3		IC COMPARATOR PRCN TO-99 PKG	01295	LM311L
A5U14	1826-0180	8	1	IC CONV 8-B-D/A 16-DIP-C PKG	04713	MC1408L-8
A5U15	1826-0081	8	3	IC OP AMP WB TO-99 PKG	27014	LM318H
A5U16	1826-0081	8		IC OP AMP WB TO-99 PKG	27014	LM318H
A5U17	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U18	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A5U19	1820-1208	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A5U20	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U21	1820-1447	2	3	IC TTL LS 16-BIT STAT RAM 45-NS 3-S	01295	SN74LS670N
A5U22	1820-1447	2		IC TTL LS 16-BIT STAT RAM 45-NS 3-S	01295	SN74LS670N
A5U23	1820-1447	2		IC TTL LS 16-BIT STAT RAM 45-NS 3-S	01295	SN74LS670N
A5U24	1820-1112	8	6	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A5U25	1820-1902	0	1	IC DRVR TTL DUAL	01295	SN75363N
A5U26	1826-0458	5		IC OP AMP TO-99 PKG	27014	LF255H
A5U27	1820-1491	6	2	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A5U28	1820-1491	6		IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A5U29	1820-0579	9	2	IC MV TTL MONOSTBL RETRIG DUAL	01295	SN74123N
A5U30	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A5U31	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A5U32	1826-0026	3		IC COMPARATOR PRCN TO-99 PKG	01295	LM311L
A5VR1	1902-0625	0	1	DIODE-ZNR 1N829 6.2V 5% DO-7 PD=.25W	04713	1N829
A5VR2	1902-0025	4	1	DIODE-ZNR 10V 5% DO-35 PD=.4W TC=+.06%	28480	1902-0025
A5VR3	1902-0600	7	1	DIODE-ZNR 1N827 6.2V 5% DO-7 PD=.4W	24046	1N827
A6	00853-60005	8	1	XYZ AMPLIFIER ASSEMBLY	28480	00853-60005
A6C1	0140-0191	0	1	CAPACITOR-FXD 56PF +-5% 300VDC MICA	72136	DM15E560J0300WV1CR
A6C2	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A6C3	0140-0199	6	2	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A6C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C5	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C7	0140-0199	6		CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A6C8	0160-4300	7	4	CAPACITOR-FXD 1PF +-.25PF 200VDC CER	28480	0160-4300
A6C9	0160-5108	9		CAPACITOR-FXD .01UF +-10% 500VDC CER	28480	0160-5108
A6C10	0160-5108	9		CAPACITOR-FXD .01UF +-10% 500VDC CER	28480	0160-5108

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6C11	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C12	0160-4388	7		CAPACITOR-FXD 10PF +-.25PF 200VDC CER	28480	0160-4388
A6C13	0160-5188	9		CAPACITOR-FXD .01UF +-10% 500VDC CER	28480	0160-5188
A6C14	0160-5188	9		CAPACITOR-FXD .01UF +-10% 500VDC CER	28480	0160-5188
A6C15	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C16	0160-4388	7		CAPACITOR-FXD 10PF +-.25PF 200VDC CER	28480	0160-4388
A6C18	0160-5188	9		CAPACITOR-FXD .01UF +-10% 500VDC CER	28480	0160-5188
A6C19	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C20	0160-4388	7		CAPACITOR-FXD 10PF +-.25PF 200VDC CER	28480	0160-4388
A6C22	0160-5188	9		CAPACITOR-FXD .01UF +-10% 500VDC CER	28480	0160-5188
A6C23	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C24	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C30	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C44	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C45	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C46	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C47	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C48	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A6C49	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C50	0160-2055	*	5	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C51	0160-3873	1	1	CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A6C52	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C53	0140-4535	4	1	CAPACITOR-FXD 10F +-10% 50VDC CER	28480	0140-4535
A6C54	0160-2308	5	1	CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2308
A6C55	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C58	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C59	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C60	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C61	0121-0059	7	1	CAPACITOR-V TRMR-CER 2-10PF 350V PC MTG	52763	304SP+ 2/10PF 500
A6C62	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C63	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C64	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C65	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C66	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C67	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C68	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C69	0160-5214	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5214
A6C70	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C71	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C72	0160-4804	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4804
A6C73	0160-4804	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4804
A6C74	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C77	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C78	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C79	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C80	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C81	0160-4804	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4804
A6C82	0160-4804	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4804
A6C83	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C84	0160-4804	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4804
A6C85	0160-4804	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4804
A6C86	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A6C87	0160-4804	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4804
A6C88	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C89	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C100	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C101	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C102	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C103	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C104	0160-4719	8	1	CAPACITOR-FXD 15PF +-5% 100VDC CER TC=0	28480	0160-4719
A6CR1	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR11	1901-0096	7	6	DIODE-SWITCHING 120V 50MA 10NS	28480	1901-0896A
A6CR12	1901-0028	8		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR13	1901-0028	8		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR15	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR18	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6CR19	1901-0896	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0896
A6CR20	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR21	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR24	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR26	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR28	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR29	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR30	1901-0896	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0896
A6CR31	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR32	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR33	1901-0896	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0896
A6CR34	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR35	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR36	1901-0896	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0896
A6CR37	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR38	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6CR39	1901-0896	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0896
A6CR40	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A6E1	9170-0847	3	1	CORE-SHIELDING BEAD	99114	56-590-A6A3B PARYLENE COATED
A6J1	1251-7678	6	1	CONNECTOR-HEADER 4 M 29	28480	1251-7678
A6L1	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L2	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L3	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L4	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L5	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L6	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L7	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L9	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L10	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6L11	9140-0210	1		INDUCTOR RF-CH MLD 100UH 5% .166DIA .385LG	28480	9140-0210
A6MP1	1205-0173	5		INSULATOR-XSTR TAB GL	28480	1205-0173
A6MP2	1205-0095	8		HEAT SINK SGL 10-32X0.39"LG	30161	6030B
A6MP3	0360-0079	5	3	PLUG-HOLE DBR-HD FOR .312" R-HOLE NYL	28480	0360-0079
A6MP4	1400-0071	6		PIN-ROLL .062"-38-STA .25"LG-LB RC-CD	28480	1400-0071
A6MP5	4040-0755	2	3	EXTR RC DR VIO POLYC .062"SQ-INSUL	28480	4040-0755
A6Q1	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q2	1854-0909	9	2	TRANSISTOR NPN 2N6439 SI TO-18 PD=360MW	28480	1854-0909
A6Q3	1853-0007	7	16	TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q4	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q5	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q6	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q7	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q8	1854-0523	4	4	TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0523
A6Q9	1854-0523	4		TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0523
A6Q10	1854-0909	9		TRANSISTOR NPN 2N6439A SI TO-18 PD=360MW	28480	1854-0909
A6Q11	1853-0036	2	2	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A6Q12	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q13	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q14	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q15	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q16	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q17	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q18	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q19	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q20	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q21	1853-0038	4	5	TRANSISTOR PNP SI TO-39 PD=1W FT=180MHZ	28480	1853-0038
A6Q22	1853-0038	4		TRANSISTOR PNP SI TO-39 PD=1W FT=180MHZ	28480	1853-0038
A6Q23	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q24	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q25	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q26	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q27	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q28	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q29	1853-0038	4		TRANSISTOR PNP SI TO-39 PD=1W FT=180MHZ	28480	1853-0038
A6Q30	1853-0038	4		TRANSISTOR PNP SI TO-39 PD=1W FT=180MHZ	28480	1853-0038
A6Q31	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q32	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A6Q33	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q34	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q35	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q36	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A6Q37	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q38	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q39	1854-0523	4		TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0523
A6Q40	1854-0967	0	2	TRANSISTOR NPN 2N2484 TO-18 PD=360MW	28480	1854-0967

See introduction to this section for ordering information
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6A1	1854-0907	0		TRANSISTOR NPN SI PD=500MW	28480	1854-0907
A6A2	1854-0523	4		TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0523
A6A3	1853-0330	4		TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ	28480	1853-0330
A6A4	1854-0419	7	2	TRANSISTOR NPN SI TO-39 PD=1W FT=200MHZ	28480	1854-0419
A6A5	1854-0419	7		TRANSISTOR NPN SI TO-39 PD=1W FT=200MHZ	28480	1854-0419
A6A6	1853-0330	4		TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ	28480	1853-0330
A6R1	0757-0270	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A6R2	2100-3353	B		RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	28480	2100-3353
A6R3	0757-0459	7	4	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A6R4	2100-3351	6	3	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A6R5	0757-0420	3		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A6R6	0698-0442	1	1	RESISTOR 4.42K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4421-F
A6R7	0757-0440	1	5	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A6R8	0757-0289	2		RESISTOR 11.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1132-F
A6R9	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-5110-F
A6R10	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R11	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A6R12	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R13	0757-0279	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A6R14	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R15	0757-0394	0	10	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A6R16	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A6R17	0757-0417	0	4	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-5620-F
A6R18	0757-0417	0		RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-5620-F
A6R19*	0698-3136	8	4	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1202-F
A6R20	2100-3352	7		RESISTOR-TRMR 2K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A6R21*	0757-0442	9	40	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R22	0698-8804	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R23	0698-8804	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R24	0698-8804	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R25	0698-8804	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R26	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R27	0757-1094	9		RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A6R28	0698-4434	0	4	RESISTOR 2.26K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2261-F
A6R29*	0757-0419	2	1	RESISTOR 3.32K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3321-F
A6R30	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A6R31	0698-4431	8		RESISTOR 2.26K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2261-F
A6R32	0757-0419	0	2	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-6810-F
A6R33	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R34*	0757-0280	1	5	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A6R35	0757-0405	6		RESISTOR 133K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R36	0757-0460	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R37	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A6R38	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A6R41*	0698-3134	6		RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1202-F
A6R41A	0698-3157	3	7	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A6R42	0757-0417	0		RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-5620-F
A6R43	0757-0417	0		RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-5620-F
A6R44	0698-8814	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R45	0698-8814	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R46	0698-8814	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R47	0698-8804	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R48	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A6R49	0757-1094	9		RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A6R50*	0757-0420	1	1	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A6R52	0698-4431	8		RESISTOR 2.26K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2261-F
A6R53	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-6810-F
A6R54	0698-4433	8		RESISTOR 2.26K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2261-F
A6R55	0757-0460	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R56	0757-0439	4	3	RESISTOR 4.02K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4021-F
A6R57	0698-3417	0	4	RESISTOR 25.5K 1% .5W F TC=0+-100	28480	0698-3417
A6R58	0757-0456	9	4	RESISTOR 2MK 1% .5W F TC=0+-100	28480	0757-0456
A6R59	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R60	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A6R61	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A6R62	0698-3486	5	5	RESISTOR 1.33K 1% .5W F TC=0+-100	28480	0698-3486
A6R63	0757-0440	1		RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A6R64	0757-0439	4		RESISTOR 4.02K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4021-F
A6R65	0698-3417	8		RESISTOR 25.5K 1% .5W F TC=0+-100	28480	0698-3417
A6R66*	0757-0456	9		RESISTOR 2MK 1% .5W F TC=0+-100	28480	0757-0456
A6R67	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R68	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A6R69	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A6R70	0698-3486	5		RESISTOR 1.33K 1% .5W F TC=0+-100	28480	0698-3486
A6R71	0757-0440	1		RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A6R73	0698-3417	8		RESISTOR 25.5K 1% .5W F TC=0+-100	28480	0698-3417

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R74	0757-0856	9		RESISTOR 75K 1% .5W F TC=0+-100	28480	0757-0856
A6R75	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5111-F
A6R76	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R77	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R78	0698-3406	5		RESISTOR 1.33K 1% .5W F TC=0+-100	28480	0698-3406
A6R79	0757-0468	1		RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-TO-6192-F
A6R81	0698-3417	8		RESISTOR 93.1K 1% .5W F TC=0+-100	28480	0698-3417
A6R82	0757-0856	9		RESISTOR 75K 1% .5W F TC=0+-100	28480	0757-0856
A6R83	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5111-F
A6R84	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R85	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R86	0698-3406	5		RESISTOR 1.33K 1% .5W F TC=0+-100	28480	0698-3406
A6R88	0698-8826	3	2	RESISTOR 825K 1% .125W F TC=0+-100	28480	0698-8826
A6R89	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5112-F
A6R90	0698-8815	8		RESISTOR 1.96M 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R92	0698-8826	3		RESISTOR 825K 1% .125W F TC=0+-100	28480	0698-8826
A6R93	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5112-F
A6R106	0698-8815	8		RESISTOR 1.96M 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R107	0698-3154	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1472-F
A6R110	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2871-F
A6R111	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R112	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1211-F
A6R113	0757-0442	9		RESISTOR 10K 1% .25W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R114	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R115	0757-0443	0	1	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1102-F
A6R116	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R117	0757-0280	3		RESISTOR 1K 1% .5W F TC=0+-100	24546	C4-1/8-TO-1001-F
A6R118	0757-0289	2		RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A6R119	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A6R120	0757-0280	7	3	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A6R121	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1471-F
A6R122	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R123	0698-0085	2	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
A6R124	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A6R125	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A6R126	0698-3447	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A6R127	0698-0085	2		RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
A6R128	0757-0280	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A6R129	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A6R130	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R132	0698-3438	3	1	RESISTOR 147 1% .125W F TC=0+-100	24546	C4-1/8-TO-147R-F
A6R133	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-100-F
A6R134	0757-0418	7		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-6190-F
A6R135	2100-3273	1		RESISTOR-TRMR 2K 10% C SIDE-ADJ 1 TRN	28480	2100-3273
A6R136	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A6R137	0698-3162	0		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4642-F
A6R138	0698-3418	9	3	RESISTOR 26.1K 1% .5W F TC=0+-100	28480	0698-3418
A6R139	0698-3152	8		RESISTOR 3.40K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3401-F
A6R140	0757-0041	2	2	RESISTOR 12.1K 1% .5W F TC=0+-100	28480	0757-0041
A6R141	0698-3419	0	2	RESISTOR 31.6K 1% .5W F TC=0+-100	28480	0698-3419
A6R142	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R143	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R144	0698-3413	4	4	RESISTOR 13.3K 1% .5W F TC=0+-100	28480	0698-3413
A6R145	0698-3413	4		RESISTOR 13.3K 1% .5W F TC=0+-100	28480	0698-3413
A6R146	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5111-F
A6R149	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3161-F
A6R150	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1211-F
A6R151	2100-3332	7		RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3332
A6R152	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A6R153	2100-3207	1	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	28480	2100-3207
A6R154	0698-3418	9		RESISTOR 26.1K 1% .5W F TC=0+-100	28480	0698-3418
A6R155	0698-3152	8		RESISTOR 3.40K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3401-F
A6R156	0757-0041	2		RESISTOR 12.1K 1% .5W F TC=0+-100	28480	0757-0041
A6R157	0698-3419	0		RESISTOR 31.6K 1% .5W F TC=0+-100	28480	0698-3419
A6R158	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R159	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
A6R160	0698-3413	4		RESISTOR 13.3K 1% .5W F TC=0+-100	28480	0698-3413
A6R161	0698-3413	4		RESISTOR 13.3K 1% .5W F TC=0+-100	28480	0698-3413
A6R162	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-100-F
A6R163	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-100-F
A6R166	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-100-F
A6R167	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-100-F
A6R168	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-100-F
A6R169	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-100-F
A6R172	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R173	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R174	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A6R175	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A6R176	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R177	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R178	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R179	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A6R180	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A6R181	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	28480	0757-0200
A6R188	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A6R189	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A6R190	0698-3458	9	1	RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4222-F
A6R191	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3161-F
A6TP1	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP2	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP3	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP4	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP5	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP6	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP7	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP8	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP9	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP10	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP11	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP12	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP13	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP14	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP15	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP16	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6TP17	0360-0535	0		TERMINAL, TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6U1	1826-0061	0		IC OP AMP WI TO-99 PKG	27014	LM108H
A6U2	1826-0417	6	1	IC SWITCH ANLG QUAD 1A-DIP-C PKG	27014	DG133DJ
A6U3	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A6U4	1826-0618	1	1	IC MULTIPLXR A QUAD ANLG DUAL 1A-DIP-C	04713	MC14016CP
A6U5	1826-0367	5	1	IC CONVRSN V TO I/I TO V	04713	MC1408L6
A6VR2	1902-0049	2		DIODE-ZNR 6.19V 5% DO-35 PD=.4W	28480	1902-0049
A6VR6	1902-0049	2		DIODE-ZNR 6.19V 5% DO-35 PD=.4W	28480	1902-0049
A7	00853-60001	1	1	PROCESSOR ASSEMBLY	28480	00853-60001
A7C1	0180-2028	6	1	CAPACITOR-FXD 220UF +-10% 35VDC TA	56289	150D227X9035B2
A7C2	0140-0205	3	1	CAPACITOR-FXD 330PF +-5% 300VDC CER 0+ 30	28480	0140-0205
A7C3	0180-0114	1		CAPACITOR-FXD 6.8UF +-10% 20VDC TA	56289	150D685X9020B2
A7C4	0180-0791	3		CAPACITOR-FXD 10UF +-10% 35VDC TA	56289	150D106X9035B2
A7C5	0160-2199	9	1	CAPACITOR-FXD 300PF +-5% 300VDC MICA	28480	0160-2199
A7C6	0140-0207	3	1	CAPACITOR-FXD 330PF +-5% 300VDC MICA	28480	0140-0207
A7C7	0160-4084	8	29	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C8	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C9	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C10	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C11	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C12	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C13	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C14	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C15	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C16	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C17	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C18	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C19	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C20	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C21	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C22	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C23	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C24	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C25	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C26	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C27	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C28	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C29	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C30	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C31	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C32	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C33	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C34	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A7C35	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A7C36	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7CR1	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A7E1	1251-4707	2	1	SHUNT-DIP 8-POSITION	28480	1251-4707
A7E2	1258-0141	8	1	JUMPER-REM	28480	1258-0141
A7J1	1200-0687	0	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0687
A7J2	1251-6067	5	1	CONNECTOR 60-PIN M POST TYPE	28480	1251-6067
A7J3	1251-5651	3	1	CONNECTOR 34-PIN M POST TYPE	28480	1251-5651
A7J4	1251-7819	7	1	CONNECTOR-HEADER 4 M 2R	28480	1251-7819
A7L2	9100-1708	6		CHOKE-MODE BAND 2MAX=600 OHMS 100 MHZ	02114	VK200 20/4D
A7MP1	0380-0458	0	3	SPACER-RVT-DN .437-IN-LG .152-IN-ID	28480	0380-0458
A7R1	0698-3440	7		RESISTOR 19K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A7R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R3	0698-3162	8		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A7R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R5	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R6	0698-3260	9		RESISTOR 464H 1% .125W F TC=0+-100	28480	0698-3260
A7R7	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R8	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R10	0757-0430	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R11	0757-0443	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A7R12	0698-3444	1	1	RESISTOR 31K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A7R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7S1	3101-2521	3	2	SWITCH-RKR DIP-RKR-ASSY .05A 30VAC/DC PC	28480	3101-2521
A7TP1	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP2	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP3	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP4	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP5	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP6	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP7	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP8	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP9	0360-0535	8		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7U1	1820-0579	9		IC MV TTL MONOSTBL,RETRIG DUAL	01295	SN74123N
A7U2	1810-0264	8	4	NETWORK-RES 8-DIP10.4K OHM X 7	01121	208A103
A7U3	1820-1917	1	5	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A7U4	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A7U5	1810-0264	8		NETWORK-RES 8-DIP10.4K OHM X 7	01121	208A103
A7U6	1818-0492	8	6	IC NMOS 409A (4K) STAT RAM 200-NS 5-V	34649	P2114A-4
A7U7	1818-0492	8		IC NMOS 409A (4K) STAT RAM 200-NS 5-V	34649	P2114A-4
A7U8	1818-0492	8		IC NMOS 409A (4K) STAT RAM 200-NS 5-V	34649	P2114A-4
A7U9	1818-0492	8		IC NMOS 409A (4K) STAT RAM 200-NS 5-V	34649	P2114A-4
A7U10	1818-0492	8		IC NMOS 409A (4K) STAT RAM 200-NS 5-V	34649	P2114A-4
A7U11	1818-0492	8		IC NMOS 409A (4K) STAT RAM 200-NS 5-V	34649	P2114A-4
A7U12	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A7U13	1810-0264	8		NETWORK-RES 8-DIP10.4K OHM X 7	01121	208A103
A7U14	1820-2483	8	1	IC RCVR TTL LS BUS OCTL	01295	SN75161N
A7U15	1820-1216	3	3	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A7U16	1820-1144	6	4	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A7U17	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A7U18	1820-1205	6	1	IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
A7U19	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A7U20	1820-2875	4	3	IC MISC TTL LS	01295	SN74LS245N
A7U21	1820-2875	4		IC MISC TTL LS	01295	SN74LS245N
A7U22	1820-2875	4		IC MISC TTL LS	01295	SN74LS245N
A7U23	1820-2405	0	1	IC RCVR TTL LS DUB OCTL	01295	SN75150N
A7U24	1820-2740	8	1	IC-0291A C MPIB	28480	1820-2740
A7U25	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A7U26	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A7U27	1820-1909	7	1	IC CNTR TTL LS DIV DUAL 4-BIT	02263	74LS393PC
A7U28	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A7U29	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A7U30	1820-1729	3	1	IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
A7U31	1820-1975	1	2	IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
A7U32	1820-1975	1		IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
A7U33	00853-80001	6	1	IC-ROM PROGRAM 2K X 8	28480	00853-80001
A7U34	00853-80002	7	1	IC-ROM PROGRAM 8K X 8	28480	00853-80002
A7U35	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A7U36	1820-1435	8	3	IC CNTR TTL LS DIV UP/DOWN SYNCHRO	01295	SN74LS669N
A7U37	1820-1438	1	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A7U38	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A7U39	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A7U40	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7U41	1826-1430	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A7U42	1826-1430	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A7U43	1826-1112	0		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A7U44	1826-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS [illegible]
A7U45	1826-1917	1		IC I/R TTL LS LINE DRVR OCTL	01295	SN74LS[illegible]N
A7U46	1826-1917	1		IC DCR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A7U47	1826-1112	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A7U48	1826-1991	1	1	IC CNTR TTL LS DECD DUAL 4-BIT	01295	SN74LS393N
A7U49	1826-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A7U50	1826-2589	5	1	IC-6502B C MPU	20480	1826-2589
A7U51	1810-0287	9	2	NETWORK-RES 8-DIP2P,8K OHM X 7	81121	288A223
A7U52	1810-0287	9		NETWORK-RES 8-DIP2P,8K OHM X 7	81121	288A223
A7U53	1826-0384	2	1	IC COMPARATOR DF QUAD 14-DIP-C PKG	27014	LM339AJ
A7U54	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A7U55	1820-1144	4		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A7U56	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS60N
A7U57	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A7U58	1820-1144	9		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A7U59	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A7U60	1820-1435	8		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
A7UA1	1820-1435	8		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
A7VR1	1902-3059	8		DIODE-ZNR 3.83V 5% DO-35 PD=.4W	28480	1902-3059
A7XA1	1200-0641	1	1	SOCKET-IC 24-CONT DIP DIP SLDR	28480	1200-0641
A7Y1	1813-0270	2	1	CRYSTAL-CLOCK-OSCILLATOR	28480	1813-0270
A8	00853-60012	7	1	PLUG-IN POWER SUPPLY ASSEMBLY	28480	00853-60012
A8C1	0140-0204	4	2	CAPACITOR-FXD .033UF +-10% 500VDC CER	51642	500-503F-X7R-333K
A8C2	0160-2933	2	1	CAPACITOR-FXD 80UF+50-10% 450VDC AL	28480	0160-2933
A8C3	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	28480	0160-4299
A8C4	0140-0204	4		CAPACITOR-FXD .033UF +-10% 500VDC CER	51642	500-503F-X7R-333K
A8C5	0160-3214	6	2	CAPACITOR-AL 4300UF 50VDC	28480	0160-3214
A8C6	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A8C7	0180-0374	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A8C8	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A8C9	0160-3214	6		CAPACITOR-FXD 4000UF +75-10% 50VDC AL	28480	0160-3214
A8C10	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A8C11	0180-0374	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A8C12	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A8C13	0160-4002	8		CAPACITOR-FXD .22UF +-10% 100VDC CER	28480	0160-4002
A8C14	0160-4002	8		CAPACITOR-FXD .22UF +-10% 100VDC CER	28480	0160-4002
A8C15	0160-4002	8		CAPACITOR-FXD .22UF +-10% 100VDC CER	28480	0160-4002
A8C16	0160-4002	8		CAPACITOR-FXD .22UF +-10% 100VDC CER	28480	0160-4002
A8C17	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A8CR1	1901-0034	5	4	DIODE-HV RECT 1KV 600MA DO-29	28480	1901-0034
A8CR2	1901-0034	5		DIODE-HV RECT 1KV 600MA DO-29	28480	1901-0034
A8CR3	1901-0034	5		DIODE-HV RECT 1KV 600MA DO-29	28480	1901-0034
A8CR4	1901-0034	5		DIODE-HV RECT 1KV 600MA DO-29	28480	1901-0034
A8CR5	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A8CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR9	1901-0418	7	4	DIODE-PWR RECT 400V 1.5A	28480	1901-0418
A8CR10	1901-0418	7		DIODE-PWR RECT 400V 1.5A	28480	1901-0418
A8CR11	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A8CR12	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A8CR13	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A8CR14	1901-0418	7		DIODE-PWR RECT 400V 1.5A	28480	1901-0418
A8CR15	1901-0418	7		DIODE-PWR RECT 400V 1.5A	28480	1901-0418
A8CR16	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A8CR17	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A8CR18	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A8DB1	1990-0487	7		LED-LAMP LUM-INT=MCD IF=20MA-MAX BVR=5V	28480	5082-4504
A8DB2	1990-0487	7		LED-LAMP LUM-INT=MCD IF=20MA-MAX BVR=5V	28480	5082-4504
A8DB3	1990-0487	7		LED-LAMP LUM-INT=MCD IF=20MA-MAX BVR=5V	28480	5082-4504
A8F1	2110-0333	9		FUSE 1.5A 125V .25X.27	28480	2110-0333
A8F2	2110-0333	9		FUSE 1.5A 125V .25X.27	28480	2110-0333
A8F3	2110-0384	7	1	FUSE .062A 125V .281X.093	28480	2110-0384
A8J1	1251-4340	1	2	CONNECTOR 6-PIN M POST TYPE	28480	1251-4340
A8J2	1251-4966	9	1	CONNECTOR D-PIN M POST TYPE	28480	1251-4966
A8J3	1251-4340	1		CONNECTOR 6-PIN M POST TYPE	28480	1251-4340
A8MP1	0380-1238	4	4	STANDOFF-RVT-ON 10-HM-LG 0.17-HM-OD BRS	00000	ORDER BY DESCRIPTION
A8MP2	0515-0165	9		SCREW-MACH M3 X 0.5 12MM-LG PAN-HD	28480	0515-0165
A8MP3	0515-0211	0		SCREW-MACH M3 X 0.5 4MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A8MP4	0535-0024	9		NUT-HEX DBL-CHAM M3 X 0.5 2.4MM-THK	00000	ORDER BY DESCRIPTION
A8MP5	1200-0043	0		INSULATOR-KOIR ALUMINUM	28480	1200-0043

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8MP4	1200-0173	5		INSULATOR-MSIR DAP-GL	28480	1200-0173
A8MP7	1251-2313	4		CONNECTOR-BGL CONT BRT .04-IN-DIC-BZ RND	28480	1251-2313
A8MP8	00853-00044	9	1	HEAT SINK	28480	00853-00044
A8MP9	2A08-0129	0		SCREW-MACH 10-32 .312-IN-LG FAN-HD-POZI	00000	ORDER BY DESCRIPTION
A8MP10	00853-28029	2	1	HEAT SINK-PLUIC-IN POWER SUPPLY	28480	00853-28029
A8MP11	2190-0004	9		WASHER-LK INTLT NO.4 .115-IN-ID	28480	2190-0004
A8MP12	3050-0891	7		WASHER-FL MTLC 3.6 MM 3.3-MM-ID	28480	3050-0891
A8MP13	2190-0005	0		WASHER-LK EXT T NO. 4 .11A-IN-ID	28480	2190-0005
A8MP14	2190-0011	8		WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
A8Q1	1854-0232	2		TRANSISTOR NPN SI TO-39 PD=1W FT=15MHZ	28480	1854-0232
A8Q2	1854-0232	2		TRANSISTOR NPN SI TO-39 PD=1W FT=15MHZ	28480	1854-0232
A8Q3	1854-0232	2		TRANSISTOR NPN SI TO-39 PD=1W FT=15MHZ	28480	1854-0232
A8Q4	1854-0411	0		TRANSISTOR NPN 2N4240 SI TO-66 PD=35W	3L605	2N4240
A8Q5	1884-0201	4		THYRISTOR-SCR 2N5595 TO-220AB VRRM=100	04713	2N5595
A8Q6	1854-0232	2		TRANSISTOR NPN SI TO-39 PD=1W FT=15MHZ	28480	1854-0232
A8R1	0813-0001	6		RESISTOR 1K 0% 3W PW TC=0+-20	28480	0813-0001
A8R2	0698-3459	0	1	RESISTOR 301K 1% .125W F TC=0+-100	28480	0698-3459
A8R3	0757-0790	4	1	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A8R4	0698-3151	7		RESISTOR 2.07K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2071-F
A8R5	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A8R6	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A8R7	0698-3135	8		RESISTOR 17.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1782-F
A8R8	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A8R9	0698-3410	9		RESISTOR 26.1K 1% .5W F TC=0+-100	28480	0698-3410
A8R10	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A8R11	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A8R12	3690-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A8R13	2100-1771	8		RESISTOR-TRMR 200 5% 0W TOP-ADJ 1-TRN	28480	2100-1771
A8R14	0757-0458	4		RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A8R15	0757-0279	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A8R16	3690-3441	0	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A8R17	2100-1771	8		RESISTOR-TRMR 200 5% 0W TOP-ADJ 1 TRN	28480	2100-1771
A8R20	0757-0405	4		RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A8R19	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A8R20	0698-3168	0	1	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A8R21	0757-0428	3		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A8R22	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A8R23	0811-1732	8	1	RESISTOR 1.06 5% 3W PW TC=0+-80	28480	0811-1732
A8TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8U1	1826-0631	6		IC-350K REGATR	28480	1826-0631
A8U2	1826-0743	5	1	IC-310K MI M ADJ	28480	1826-0743
A8VR1	1902-0743	3		DIODE-ZNR 10944 11.7V 5% 20-7 PD=.5W	04713	1N744
A8VR2	1902-0071	0	1	DIODE-ZNR 5V 5% ED-10 PD=.4W TC=+.001%	28480	1902-0071
A8VR3	1902-0665	7	1	DIODE-ZNR 3V0 5% PD=5W TR=5%	28480	1902-0665
A8VR4	1902-0506	5	1	DIODE-ZNR 7.87V 2% 1W-15 PD=1W TR=.002%	28480	1902-0506
A9	8853A-60011	6	1	INTERFACE ASSEMBLY	28480	08853-60011
A9C1	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9C2	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035B2
A9C3	0160-4314	7	1	CAPACITOR-FXD .05UF +-1% 200VDC	28480	0160-4314
A9C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9C5	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035B2
A9C6	0180-0291	3		CAPACITOR-FXD 10UF+-10% 35VDC TA	56289	150D106X9035B2
A9C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9C8	0160-3456	8	1	CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-3456
A9C9	0160-3874	1	1	CAPACITOR-FXD 100PF +-10PF 300VDC CER	28480	0160-3874
A9CR1	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR2	1901-0376	6		DIODE-SW PRD 35V 50MA DO-35	28480	1901-0376
A9CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9J1	1200-0538	0	2	SOCKET-IC 14 CONT DIP-SLDR	28480	1200-0538
A9J2	1251-2565	8	1	CONNECTOR-HEADER 10 M 1R	28480	1251-2565
A9L1	9140-0144	8	3	INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.24LG	28480	9140-0144
A9L2	9140-0144	8		INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.24LG	28480	9140-0144
A9L3	9140-0144	8		INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.24LG	28480	9140-0144

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9Q1	1854-0404	8		TRANSISTOR NPN SI TO-18 PD=400MW	28480	1854-0404
A9Q2	1853-0307	7		TRANSISTOR PNP 2N4250 GP SI TO-18 PD=360MW	04713	2N4250
A9Q3	1854-0404	8		TRANSISTOR NPN SI TO-18 PD= 400MW	28480	1854-0404
A9Q4	1853-0316	1		TRANSISTOR-DUAL PNP PD=500MW	28480	1853-0316
A9Q5	1855-0270	8	2	TRANSISTOR J-FET 2N5114 P- CHAN D MODE	17856	2N5114
A9Q6	1855-0270	8		TRANSISTOR J-FET 2N5114 P- CHAN D MODE	17856	2N5114
A9Q7	1854-0404	8		TRANSISTOR NPN SI TO-18 PD= 400MW	28480	1854-0404
A9Q8	1854-0478	8		TRANSISTOR-DUAL NPN PD=?.0W	28480	1854-0478
A9R1	0698-6977	1	2	RESISTOR 33K .1% .125W F TC=0+-25	28480	0698-6977
A9R2	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A9R3	0698-6977	1		RESISTOR 33K .1% .125W F TC=0+-25	28480	0698-6977
A9R4	0698-6362	8	2	RESISTOR 1K .1% .125W F TC=0+-25	28480	0698-6362
A9R5	0757-0280	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A9R6	0757-0436	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A9R7	0757-1093	5	1	RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1093
A9R8	0698-6362	8		RESISTOR 1K .1% .125W F TC=0+-25	28480	0698-6362
A9R9	0698-6364	0	1	RESISTOR 40K .1% .125W F TC=0+-25	28480	0698-6364
A9R10	0757-0394	8		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-5101-F
A9R11	0698-6436	5		RESISTOR 1.33K 1% .5W F TC=0+-100	28480	0698-6436
A9R12	0757-0394	8		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-5101-F
A9R13	0698-6442	4		RESISTOR 42K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A9R14	0698-6376	4	2	RESISTOR 200K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-2003-B
A9R15	0698-6350	2	1	RESISTOR 100W .1% .125W F TC=0+-25	28480	0698-6350
A9R16	0698-0034	3	1	RESISTOR 9K .1% .125W F TC=0+-0	28480	0698-0034
A9R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R18	0698-0022	4	5	RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-0022
A9R19	0698-6376	4		RESISTOR 200K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-2003-B
A9R20	0757-0450	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A9R21	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R22	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A9R23	0698-0085	0		RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A9R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R25	0757-0394	8		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-5101-F
A9R26	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A9R27	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A9R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R29	0698-0027	4		RESISTOR 100 1% .125W F TC=0+-100	28480	0698-0027
A9R30	0698-6157	3		RESISTOR 15.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1542-F
A9R31	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R32	0698-0027	4		RESISTOR 100 1% .125W F TC=0+-100	28480	0698-0027
A9R33	0698-6827	4		RESISTOR 4K 1% .125W F TC=0+-100	28480	0698-6827
A9R34	0698-6827	4		RESISTOR 4K 1% .125W F TC=0+-100	28480	0698-6827
A9R35	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R36	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9R37	0757-0401	7		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-1000-F
A9R38	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A9R39	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-5110-F
A9R40	0757-0467	8	2	RESISTOR 121K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A9R45	0757-0467	8		RESISTOR 121K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A9R46	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A9R47	0698-6827	4		RESISTOR 4 MEGOHM 1% .125W	28480	0698-6827
A9S1	3101-2506	6	1	SWITCH-ROCKER DPST-NON	28480	3101-2506
A9TP1	0360-0535	0		TERMINAL TEST POINT PCB	28480	ORDER BY DESCRIPTION
A9TP2	0360-0535	0		TERMINAL TEST POINT PCB	28480	ORDER BY DESCRIPTION
A9TP3	0360-0535	0		TERMINAL TEST POINT PCB	28480	ORDER BY DESCRIPTION
A9TP4	0360-0535	0		TERMINAL TEST POINT PCB	28480	ORDER BY DESCRIPTION
A9TP5	0360-0535	0		TERMINAL TEST POINT PCB	28480	ORDER BY DESCRIPTION
A9TP6	0360-0535	0		TERMINAL TEST POINT PCB	28480	ORDER BY DESCRIPTION
A9TP7	0360-0535	0		TERMINAL TEST POINT PCB	28480	ORDER BY DESCRIPTION
A9U1	1810-0388	9	1	NETWORK-RES 14-PIN MULTI-VALUE	28480	1810-0388
A9U2	1810-0284	8		NETWORK-RES 8-PIN 8.0K OHM X 7	91121	B8K103
A9U3	1810-0185	7	1	NETWORK-RES 8-PIN 4.7K OHM X 7	91121	B4K472
A9U4	1826-0705	1		IC-9720 C2 OP AMP	01295	TL972BCLP
A9U5	1810-0371	6	1	NETWORK-RES 8-PIN 100.0K OHM X 7	91121	B100K104
A9VR1	1902-0049	2		DIODE ZNR 6.19V 5% DO-35 PD= 4W	28480	1902-0049
A10	08853-60009	2	1	HP-IB INTERCONNECT ASSEMBLY	28480	08853-60009
A10J1	1251-4848	0	1	CONNECTOR 24-PIN F MICRO RIBBON	28480	1251-4848
A10S1	3101-2501	3		SWITCH-SLIDE DPST-NON-ACTY .1A 30VAC/DC PC	28480	3101-2501

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1W1	08853-60023	0	1	CABLE ASSEMBLY-PROC-HPIB	28480	08853-60023
A11	08853-60038	5	1	PRIMARY SWITCHING ASSEMBLY	28480	08853-60018
A1S1 A1S2	3101-2552 3101-2552	0 0	2	SWITCH-SL DPDT DTD 5A 250VAC PC SWITCH-SL DPDT DTD 5A 250VAC PC	20480 20480	3101-2552 3101-2552
A12	08853-60006	9	1	MOTHERBOARD ASSEMBLY	28480	08853-60006
A12J1 A12J2 A12J3 A12J4 A12J5	1251-7684	4	1	PART OF A12W1 NOT ASSIGNED CONNECTOR-HEADER 14 H 1R NOT ASSIGNED NOT ASSIGNED	28480	1251-7684
A12J6 A12J7 A12J8 A12J9	1200-0569	0	1	SOCKET-IC 14-CONT DIP-SLDR NOT ASSIGNED PART OF A12W2 CONNECTOR 2-PIN,M POST TYPE	28480	1200-0569
A12MP1	0380-1511	6	8	STANDOFF- 4 MML M3.0	28480	0380-1511
A12W1 A12W2	08853-60021 08853-60022	8 9	1 1	CABLE ASSEMBLY-DISPLAY CONTROL CABLE ASSEMBLY-PROCESSOR/MB	28480 28480	08853-60021 08853-60022
A12XA2 A12XA4 A12XA5 A12XA6	1251-0472 1251-2035 1251-2915 1251-2915	4 9 4 4	1 1 2	CONNECTOR-PC EDGE 6-CONT/ROW 2-ROWS CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480 28480 28480 28480	1251-0472 1251-2035 1251-2915 1251-2915
A13	08853-60052	5	1	FAN MODULE ASSEMBLY	28480	08853-60052
A13W1				CABLE ASSEMBLY-FAN (P/O A13)		
A14	08853-60040	9	1	CRT ASSEMBLY (SEE FIGURE 6-4 FOR MECHANICAL PARTS)	28480	08853-60040
A14L1	01340-66501	8	1	TRACE ALIGN COIL	28480	01340-66501
A14V1	5082-6178	6	1	CRT	28480	5082-6178
A14W1				SEE FIGURE 6-4.		

See Introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	c d	Qty	Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS-ELECTRICAL		
B1	3160-0766	3	1	FAN-TDAX 36 CFM 6-16VDC	72410	3160-0766
F1	2110-0002	9	1	FUSE 2A 250V NTD 1.25X.25 UL	75915	312002
F1	2110-0001	8	1	FUSE 1A 250V NTD 1.25 X .25 UL	04400	AGC-1
FL1	9135-0038	0		LINE FILTER MODULE	28480	9135-0038
J1	1251-0137	8	1	PLUG-IN SOCKET(CONN RF F ONG NOT ARRIVED	28480	1250-1794
J2						
J3	1250-1794	3	2	HDR12 (SWEEP)(CONN RF F ONG	28480	1250-1794
J4				VERTICAL (VERT)(CONN RF F) P/O W40		
J5	1250-1794	3	1	BLANK(PNL3FT)(CONN RF F ONG	28480	1250-1794
J6				21.4MHZ IF(CONN RF) P/O W40		
S1	3103-0063	0	1	SWITCH-THRW EXD .4VDC 3A DPH-DM-RTRN	28480	3103-0063
S2	3101-0580	2	1	LINE SWITCH DW-PB DPST ALT.	28480	3101-2580
T1	00853-60040	7	1	TRANSFORMER- INCLUDED W3	28480	00853-60040
U1	0960-0635	3	1	HIGH VOLTAGE MULTIPLIER	28480	0960-0635
W1	00853-60026	3	1	CABLE ASSEMBLY-ERT(INCL J2)	28480	00853-60026
W2				CABLE ASSY-LOW VOLT PWR SPLY(P/O T1)		
W3	00853-60035	2	1	CABLE ASSY-PLUG-IN(INCL J1,J3-J6	28480	00853-60035
W4	00853-60029	4	1	CABLE ASSY-LINE PSWER(INCL S2	28480	00853-60029
W5	8120-3685	1	1	CABLE ASSY-DSPL PWR SUPPLY(FLEX	28480	8120-3685
W6	00853-60024	1	1	CABLE ASSY-INTERFACE(I&C	28480	00853-60024
W301	0160-4154	6	1	CAPACITOR-FXD .047UF +-10% (80VDC CER	28480	0160-4154
W340	00853-60027	4	1	CABLE ASSY-VERTICAL (VERT)(INCL J4	28480	00853-60027
W342	00853-60028	5	1	CABLE ASSY-21.4MHZ IF (INCL J6	28480	00853-60028

See Introduction to this section for ordering information
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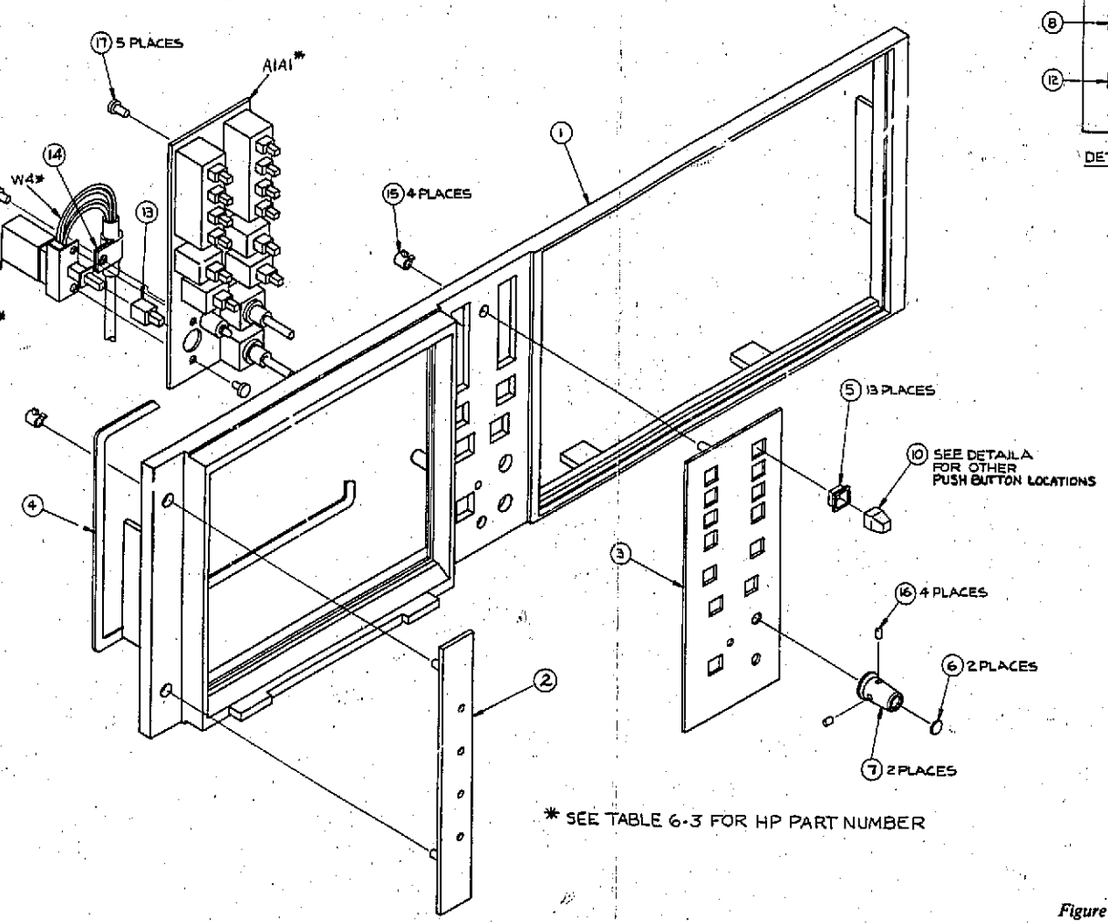
Item	HP Part Number	C D	Qty	Description	Mfr. Code	Mfr. Part Number
1	00853-20027	0	1	SUB-FRAME, FRONT	28480	00853-20027
2	00853-00003	0	1	CRT ADJUST-PANEL	28480	00853-00003
3	00853-00001	8	1	FRONT DISPLAY PANEL	28480	00853-00001
4	1520-0215	4	1	SHOCK PAD NPRN 4.5-WD 5.75-LG	28480	1520-0215
5	0370-0606	7	13	BEZEL-PUSHBUTTON 0.330-IN SQ JADE GREY	28480	0370-0606
6	0350-1012	9	2	DECAL-KB CAP 5/16 IN-SER	28480	0350-1012
7	5040-8805	0	2	KNOB, 5/16" SERIES	28480	5040-8805
8	5040-8816	3	2	PUSHBUTTON, SQUARE, MINT GREY	28480	5040-8816
9	5040-8817	4	2	PUSHBUTTON, SQUARE, JADE GREY	28480	5040-8817
10	5040-8819	6	2	PUSHBUTTON, SQUARE, WILLOW GREEN	28480	5040-8819
11	5040-8821	0	6	PUSHBUTTON, SQUARE, OLIVE GREY	28480	5040-8821
12	5041-3909	7	1	PUSHBUTTON, CHINA WHITE	28480	5041-3909
13	00853-40005	6	1	EXTENSION PUSHBUTTON	28480	00853-40005
14	1400-0017	0	1	CLAMP-CABLE .312-DIA .375-WD NYL	03480	3305 RED
15	0510-1148	2	4	RETAINER-PUSH ON KB-TO-SHFT EXT	04828	C4154-017-27
16	3030-0195	2	4	SCREW-SET 2-56 .094-IN LG	28480	3030-0195
17	0515-0211	8	5	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	28480	0515-0211
	08565-60170	5	2	KNOB ASSY: INCLUDES ITEMS 6, 7, AND 16	28480	08565-60170



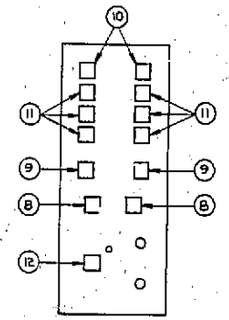


Figure 6-1. Front Panel, Parts Locations

PARTS LIST CON'T

Item	HP Part Number	C D	Qty	Description	Mfr. Code	Mfr. Part Number
1	00853-00002	9	1	REAR PANEL	28480	00853-00002
2	0380-1529	6	2	STANDOFF-HEX 6.1-MM-LG M3.5 X 0.6 THD	28480	0380-1529
3	2190-0586	2	2	WASHER-LK HLCL 4.0MM 4.1-MM-ID	28480	2190-0586
4	0535-0006	1	2	NUT-HEX DBL-CHAM M4 X 0.7 3.2MM-THK	28480	0535-0006
5	0400-0225	1	A/R	GROMMET-CHAN SERR .031-IN-GRV-WD	02201	SNGS-1
6	0515-0413	2	4	SCREW-MACH M4 X 0.7 6MM-LG PAN-HD	28480	0515-0413
7	0515-0211	8	1	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	28480	0515-0211
8	3050-0890	6	8	WASHER-FL M2.5ID	28480	3050-0890
9	0515-0739	5	2	SCREW-MACH M2.5 X 0.45 18MM-LG PAN-HD	28480	0515-0739
10	0515-0402	9	2	SCREW-MACH M2.5 X 0.45 4MM-LG PAN-HD	28480	0515-0402
11	0360-0355	2	2	TERMINAL-SLDR LUG PL-MTG FOR No. 5-SCR	04880	541
12	3050-0891	7	10	WASHER-FL MTLC 3.0MM 3.3-MM-ID	28480	3050-0891
13	2190-0584	0	6	WASHER-LK HLCL 3.0MM 3.1-MM-ID	28480	2190-0584
14	0535-0004	9	6	NUT-HEX DBL-CHAM M3 X 0.5 2.4MM-THK	28480	0535-0004
15	2110-0565	9	1	FUSEHOLDER-CAP 12A MAX FOR UL	08666	031.1666
16	2110-0566	0	1	FUSEHOLDER-EXTR POST 12A 250V	08666	031.1677
17	2110-0569	3	1	FUSEHOLDER-COMPONENT NUT THREAD M12.7	08666	0583.0016
18	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYLON	04225	TY-23M-8
19	0515-0737	3	4	SCREW-MACH M2.5 X 0.45 30MM-LG PAN-HD	28480	0515-0737
20	00853-20045	2	2	FAN HOUSING	28480	00853-20045
21	00853-00012	1	1	FINGER GUARD	28480	00853-00012
22	0624-0099	1	8	SCREW-TPG 4-40 .375-IN-LG PAN-HD-POZI	28480	0624-0099
23	0515-0772	6	2	SCREW-MACH M3 X 0.5 8MM-LG 90 DEG FLH-HD	28480	0515-0772
24	0380-1380	7	4	STANDOFF-HEX 25-MM-LG M4.0 X 0.7 THD	28480	0380-1380
25	0515-0738	4	4	SCREW-MACH M5 X 0.8 14MM-LG PAN-HD	28480	0515-0738
26	85680-00047	1	1	COVER, TRANSFORMER	28480	85680-00047
27	0390-0006	3	8	INSULATOR-FLG-BSHG,NYLON	28480	0390-0006
28	00853-00018	7	1	SHIELD, TRANSFORMER	28480	00853-00018
29	8150-3284	5	A/R	WIRE 18 AWG G/Y 300V	28480	8150-3284
30	8150-0159	7	A/R	WIRE 22 AWG W/BR/GY 300V	28480	8150-0159
31	0890-0029	0	6	TUBING-HS	28480	0890-0029
32	0890-0983	5	4	TUBING-HS	28480	0890-0983
33	1400-0017	0	1	CLAMP-CABLE .312DIA .375WD	04495	19S3-5B-RED
34	8150-0152	0	A/R	WIRE 24 AWG W 600V	28480	8150-0152
35	3050-0893	9	4	WASHER-FL MTLC 4.0MM 4.4-MM-ID	28480	3050-0893

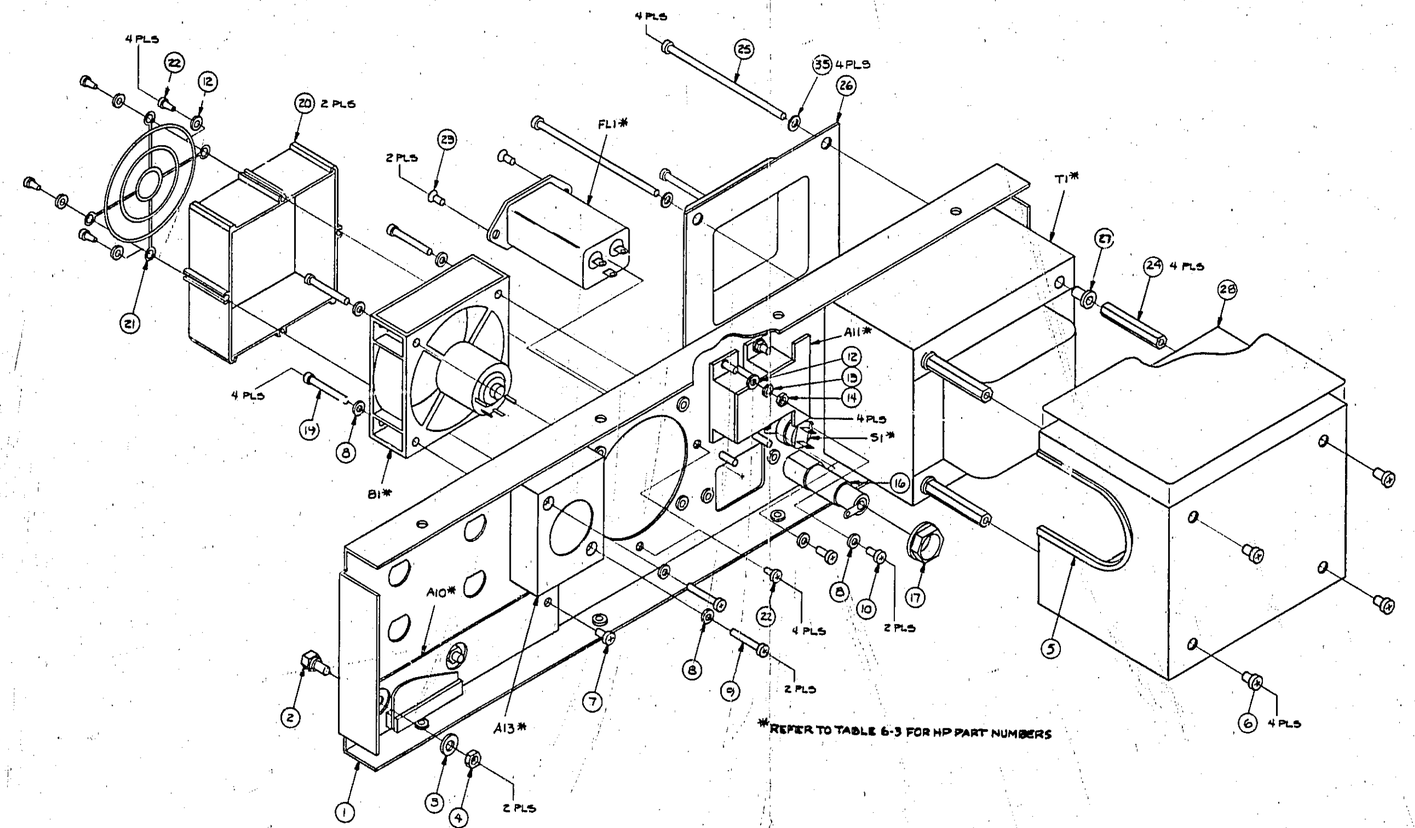


Figure 6-2. Rear Panel, Parts Locations (1 of 2)

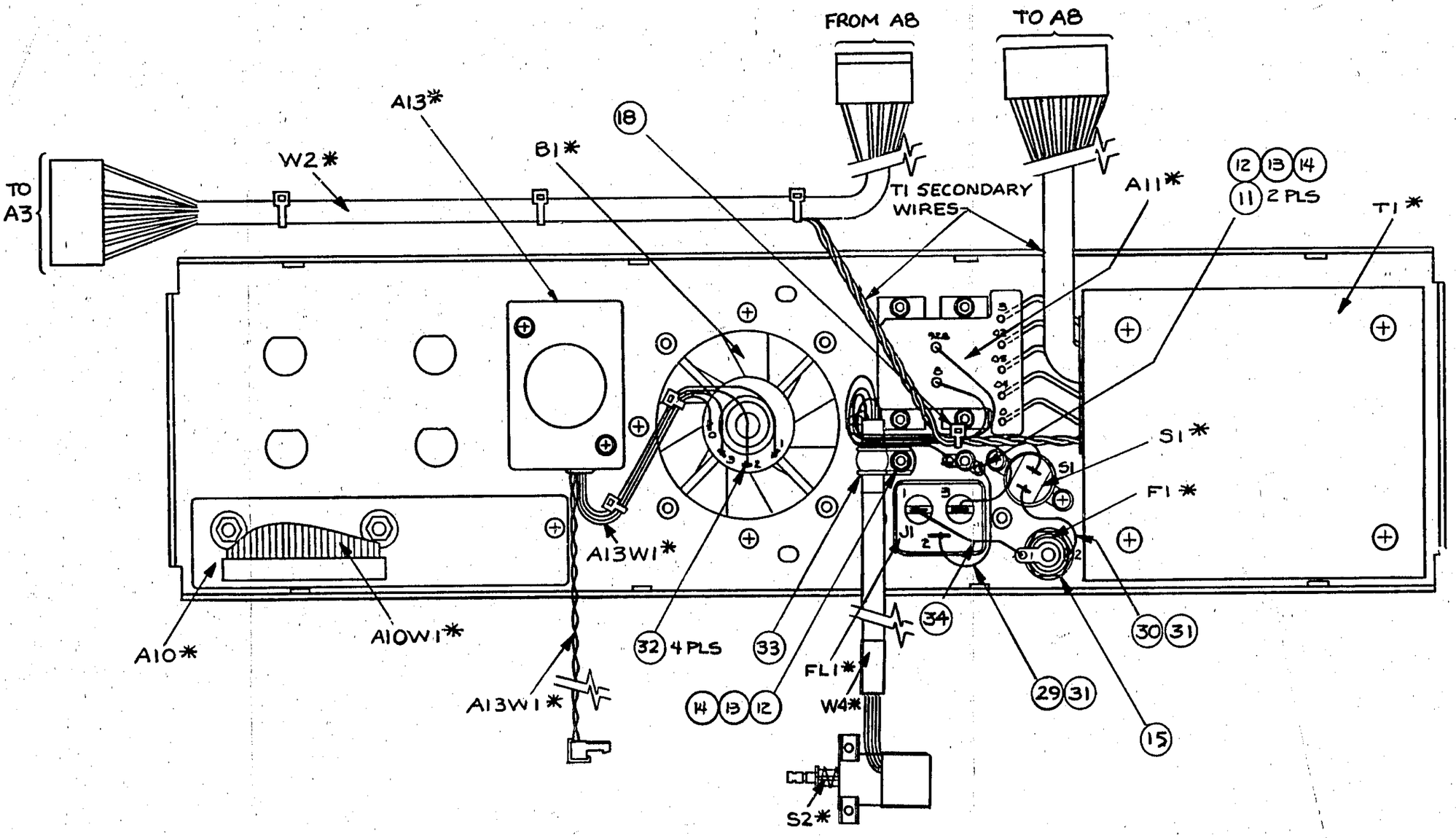


Figure 6-2. Rear Panel, Parts Locations (2 of 2)

Item	HP Part Number	C D	Qty	Description	Mfr. Code	Mfr. Part Number
1	00853-00028	9	1	BRACKET, CENTER PANEL ASSEMBLY	28480	00853-00028
2	00853-20028	1	1	SUPPORT, FRONT CENTER	28480	00853-20028
3	5020-8804	7	1	REAR FRAME	28480	5020-8804
4	00853-00025	6	1	PLUG-IN SHELF ASSEMBLY	28480	00853-00025
5	00853-00029	0	1	ENCLOSURE: HV, DATA, XYZ ASSEMBLIES	28480	00853-00029
6	00853-00010	9	1	HEATSINK PLATE	28480	00853-00010
7	00853-00011	0	1	PANEL, CRT ENCL	28480	00853-00011
8	0515-0413	2	2	SCREW-MACH M4 X 0.7 6MM-LG PAN-HD	28480	0515-0413
9	00853-00008	5	1	BRACKET, CRT	28480	00853-00008
10	00853-00030	3	1	CRT SUPPORT ASSEMBLY	28480	00853-00030
11	0515-0407	4	2	SCREW-MACH M3 X 0.5 10MM-LG PAN-HD	28480	0515-0407
12	0624-0411	1	13	SCREW-MPG 6-19 .313-IN-LG PAN-HD-POZI	28480	0624-0411
13	00853-40001	2	1	UPPER GUIDE RAIL: RIGHT SIDE	28480	00853-40001
14	00853-40002	3	1	UPPER GUIDE RAIL: LEFT SIDE	28480	00853-40002
15	00853-20025	8	1	FRAME MODULE, FRONT	28480	00853-20025
16	00853-00026	7	2	CONTACT, SPRING	28480	00853-00026
17	00853-20038	3	2	SIDE RAIL, BOTTOM	28480	00853-20038
18	00853-20039	4	2	SIDE RAIL, TOP	28480	00853-20039
19	0400-0001	1	1	GROMMET-RND .562-IN-ID .75-IN-GRV-OD	04604	1662
20	0515-0395	9	6	SCREW-MACH M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-0395
21	2580-0003	5	2	NUT-HEX-W/LKWR 8-32-THK .125-IN-THK	04805	511081800-00-0280-2580
22	0515-0211	8	33	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	28480	0515-0211
23	3050-0891	7	15	WASHER-FL MTLC 3.0 MM 3.3-MM-ID	28480	3050-0891
24	2510-0192	6	16	SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
25	0535-0004	9	2	NUT-HEX DBL-CHAM M3 X 0.5 2.4MM-THK	28480	0535-0004

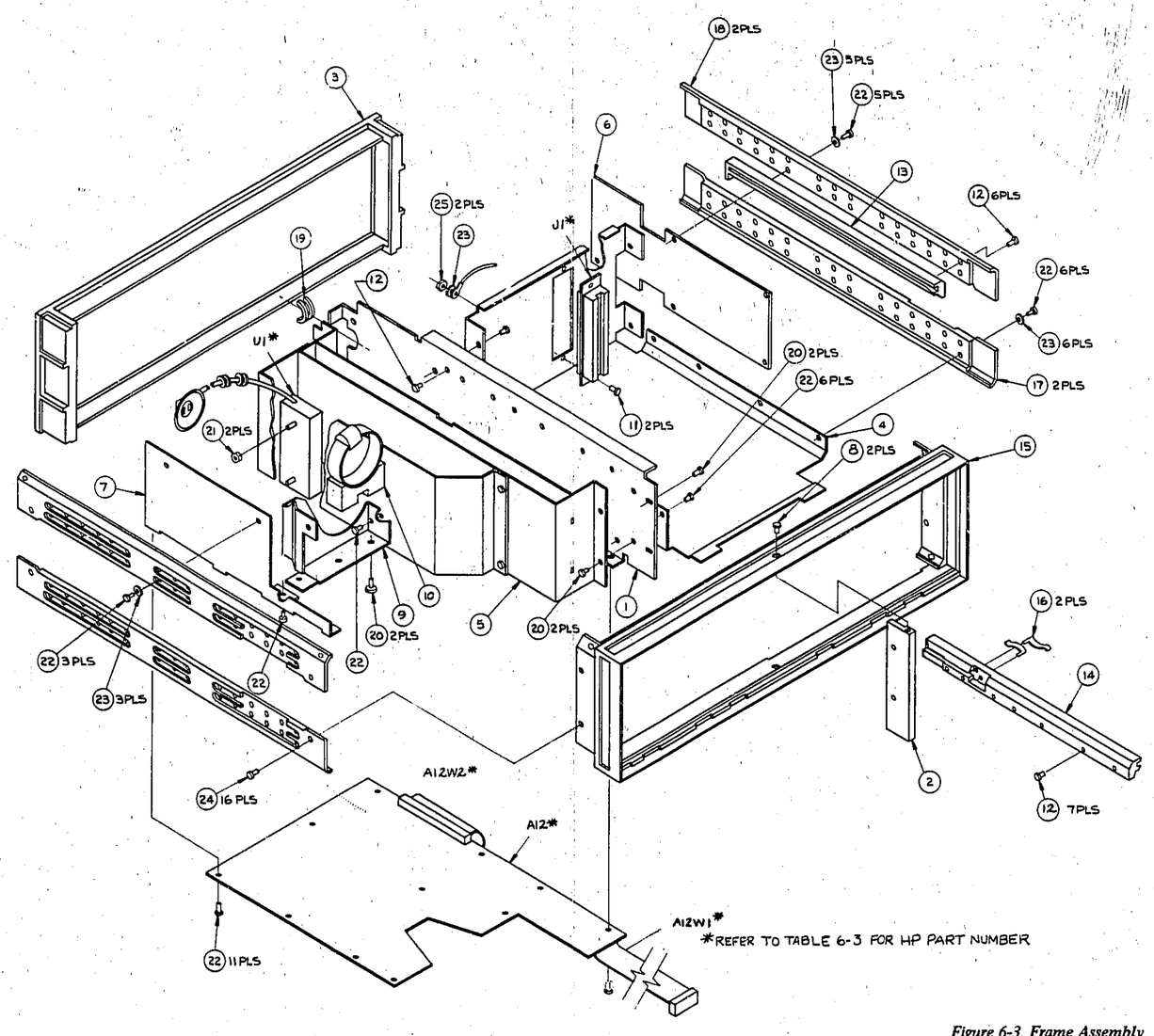
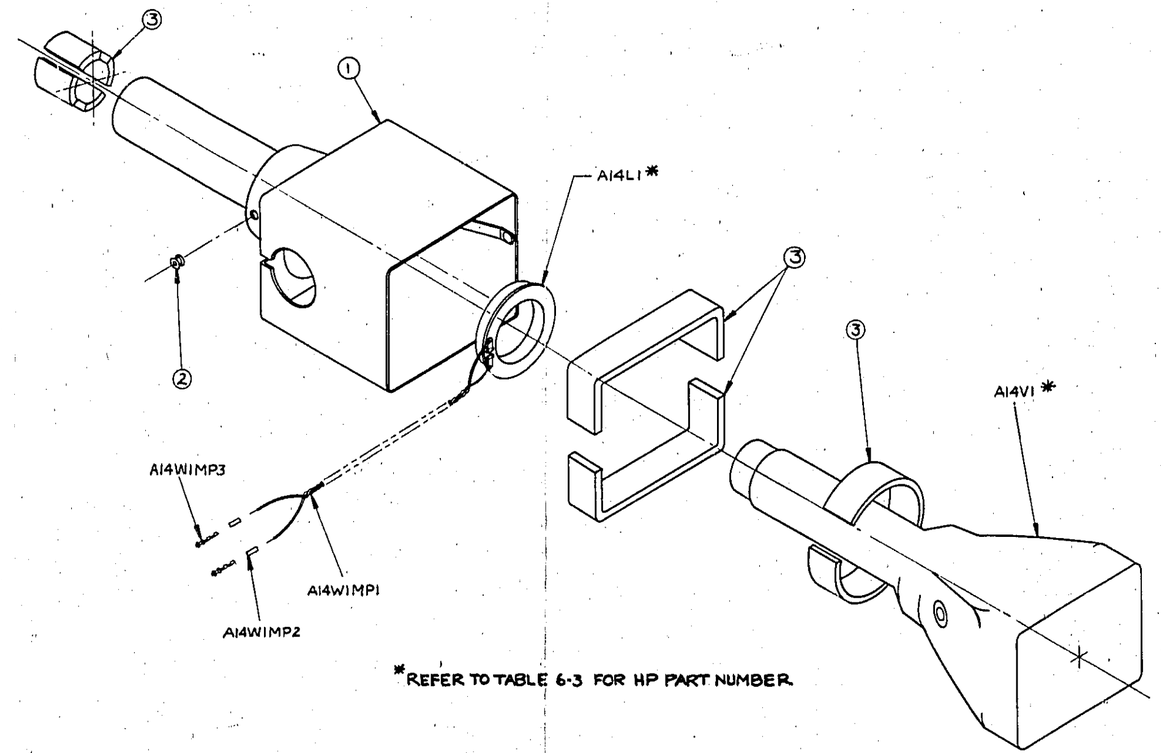


Figure 6-3. Frame Assembly, Parts Locations

Item	HP Part Number	C D	Qty	Description	Mfr. Code	Mfr. Part Number
1	00853-60051	4	1	SHIELD ASSEMBLY	28480	00853-60051
2	0400-0009	9	1	GROMMET-RND ,125-IN-ID ,25-IN-GRV-OD	01808	C250
3	0460-0114	3	A/R	TAPE-INOL 1.25-IN-W ,25-IN-T POLY-FM	05347	TESA 761-4763
A14W1MP1	8150-0149	5	A/R	WIRE 22 AWG W/BK/G 300V PVC 7 X 30 105C	28480	8150-0149
A14W1MP2	0890-0983	5	A/R	TUBING-HS ,125-D/,062-RCVP ,02-WALL	02145	RNF-100-1/8-BLK
A14W1MP3	0362-0227	1	2	CONNECTOR-SGL CONT SKT 1.14-MM-BSC-SZ	03418	02-05-5216



*REFER TO TABLE 6-3 FOR HP PART NUMBER.

Figure 6-4. CRT Assembly, Parts Locations

Item	HP Part Number	C D	Description	Mfr. Code	Mfr. Part Number
1	00853-00013	2	BOARD, INSULATOR	28480	00853-00013
2	00853-20033	8	CATCH	28480	00853-20033
3	00853-00038	1	LATCH CATCH SPRING	28480	00853-00038
4	8160-0415	9	RFI "D" STRIP CNDCT-ELSTMR AG-PL	02923	10-05-4699-140
5	0515-0795	3	SCREW-MACH M2 X 0.4 20MM-LG	28480	0515-0795
6	3050-0891	7	WASHER-FL MTLC 3.6MM 3.3-MM-ID	28480	3050-0891
7	0515-0772	6	SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-0772
8	0515-0395	9	SCREW-MACH M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-0395
9	0515-0211	8	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	28480	0515-0211
10	0515-0413	2	SCREW-MACH M4 X 0.7 6MM-LG PAN-HD	28480	0515-0413
11	00853-20024	7	SHAFT, LONG, DISPLAY ADJUST	28480	00853-20024
12	00853-20023	6	SHAFT, SHORT, DISPLAY ADJUST	28480	00853-20023
13	9135-0052	8	RFI CRT SHIELD	28480	9135-0052
14	1490-0841	7	COUPLER-RGD .375-LG BRS	28480	1490-0841
15	3030-0007	5	SCREW-SET 4-40 .125-IN-LG SMALL CUP-PT	28480	3030-0007
16	00853-00019	0	COVER-HIGH VOLTAGE	28480	00853-00019
17	00853-00024	7	HOLD DOWN, DATA/XYZ BOARDS	28480	00853-00024
18	00853-20031	6	COVER, PLUG-IN POWER SUPPLY	28480	00853-20031
19	00853-20032	7	COVER, DISPLAY POWER SUPPLY	28480	00853-20032
20	00853-20044	1	BUSHING	28480	00853-20044
21	0515-0407	4	SCREW-MACH M3 X 0.5 10MM-LG PAN-HD	28480	0515-0407
22	00853-40003	4	CRT BEZEL	28480	00853-40003
23	0515-0219	6	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FLH-HD	28480	0515-0219

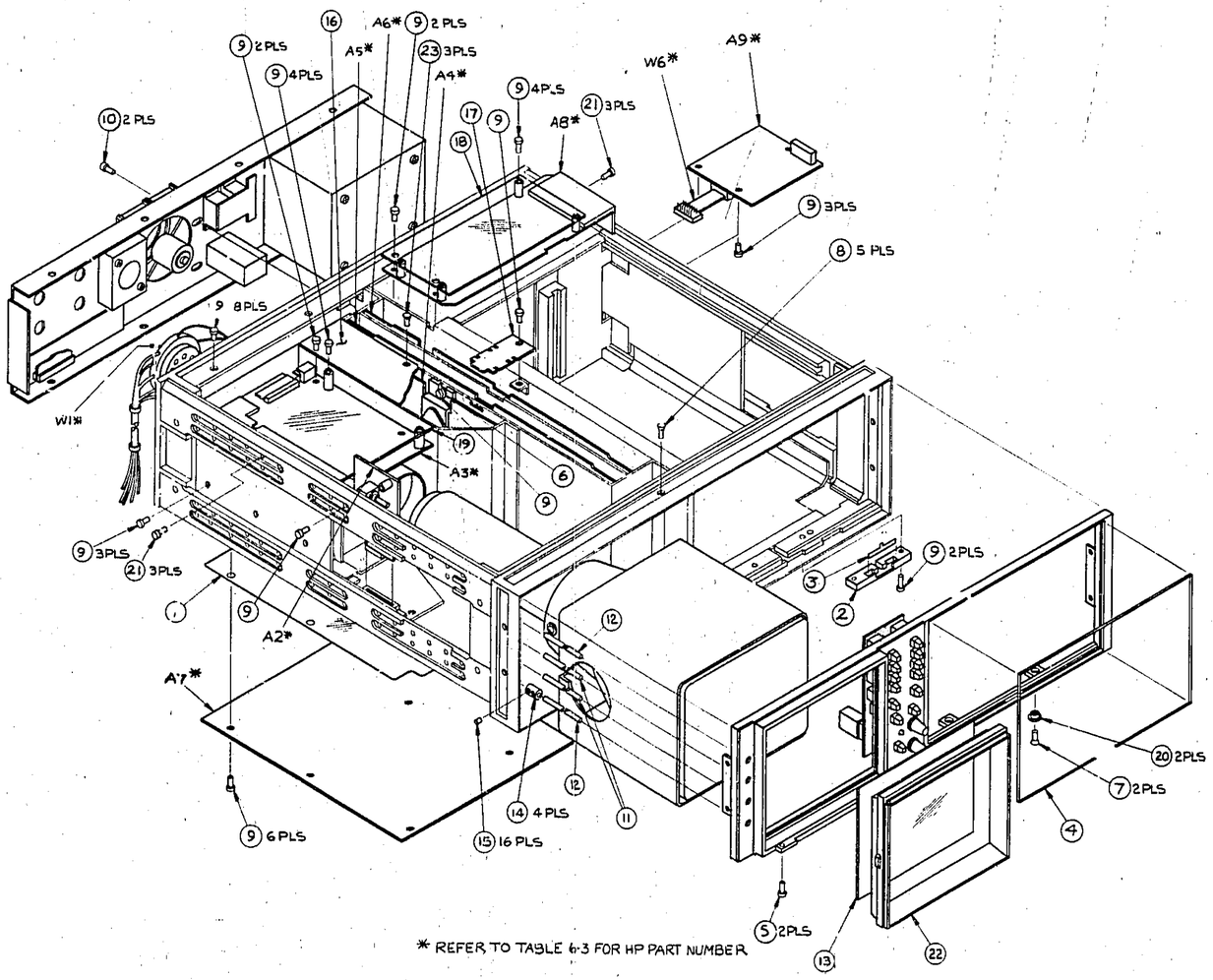


Figure 6-5. Chassis Parts

Item	HP Part Number	C D	Description	Mfr. Code	Mfr. Part Number
1	00853-40011	4	HANDLE ASSEMBLY	28480	00853-40011
2	5001-0439	8	TRIM, SIDE FRONT	28480	5001-0439
3	00853-20035	0	HANDLE, PIVOT	28480	00853-20035
4	2510-0192	6	SCREW-MACH 8-32 .25-IN-LG 100-DEG	28480	2510-0192
5	0905-0954	3	O-RING 1.489-IN-ID .07-IN-XSECT-DIA	04748	AS568-029-N11
6	00853-40007	8	COLLAR, BEZEL	28480	00853-40007
7	5020-8734	2	GEAR, RING HANDLE	28480	5020-8734
8	5020-8733	1	GEAR, HUB HANDLE	28480	5020-8733
9	1460-0604	7	SPRING	28480	1460-0604
10	2190-0586	2	WASHER-LK HLCL 4.3MM 4.1MM-ID	28480	2190-0586
11	0515-0[illegible]	8	SCREW-MACH M4 X 0.7 20MM-LG PAN-HD	28480	0515-0443
12	2360-01[illegible]	2	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	28480	2360-0121
13	5041-2642	3	TRIM CAP	28480	5041-2642
14	00853-40009	0	REAR FEET	28480	00853-40009
15	2360-0219	9	SCREW-MACH 6-32 1.375-IN-LG PAN-HD-POZI	28480	2360-0219
16	00853-00040	5	BOTTOM COVER ASSEMBLY	28480	00853-00040
17	00853-00039	2	TOP COVER ASSEMBLY	28480	00853-00039
18	8160-0410	4	RFI "D" STRIP CNDCT-ELSTMR .078-IN-WD	02923	10-05-1363-1250
19	5001-5827	8	TRIM-SD FRONT FR	28480	5001-5827
20	00853-60049	0	FRONT PANEL COVER ASSEMBLY	28480	00853-60049

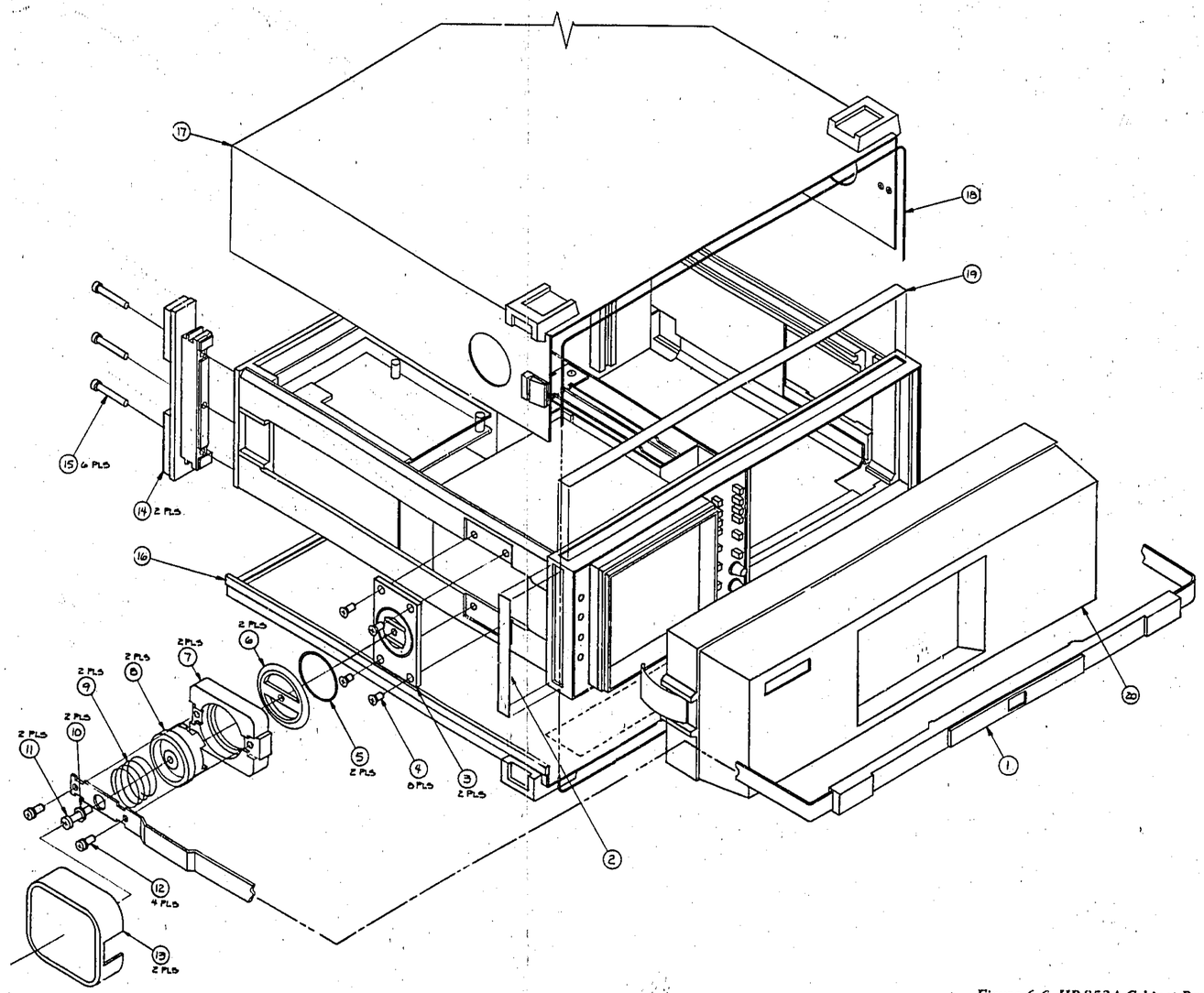


Figure 6-6. HP 853A Cabinet Parts

Item	HP Part Number	C D	Description	Mfr. Code	Mfr. Part Number
1	1460-1345	5	TILT STAND	28480	1460-1345
2	5060-9936	2	SIDE COVER WITH HANDLE	28480	5060-9936
3	5060-9911	3	SIDE COVER, PERFORATED	28480	5060-9911
4	5060-9846	3	COVER, BOTTOM	28480	5060-9846
5	5060-9834	9	COVER, TOP	28480	5060-9834
6	5060-9803	2	STRAP HANDLE	28480	5060-9803
7	5040-7220	1	COVER, STRAP HANDLE, RIGHT-REAR	28480	5040-7220
8	5040-7219	8	COVER, STRAP HANDLE, RIGHT-FRONT	28480	5040-7219
9	2680-0172	1	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
10	5040-7221	2	FOOT, REAR	28480	5040-7221
11	2360-0195	0	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	28480	2360-0195
12	5040-7201	8	FOOT, BOTTOM	28480	5040-7201
13	5060-0089	8	KIT, FRONT HANDLES	28480	5060-0089
14	5040-7202	9	STRIP, TRIM TOP	28480	5040-7202

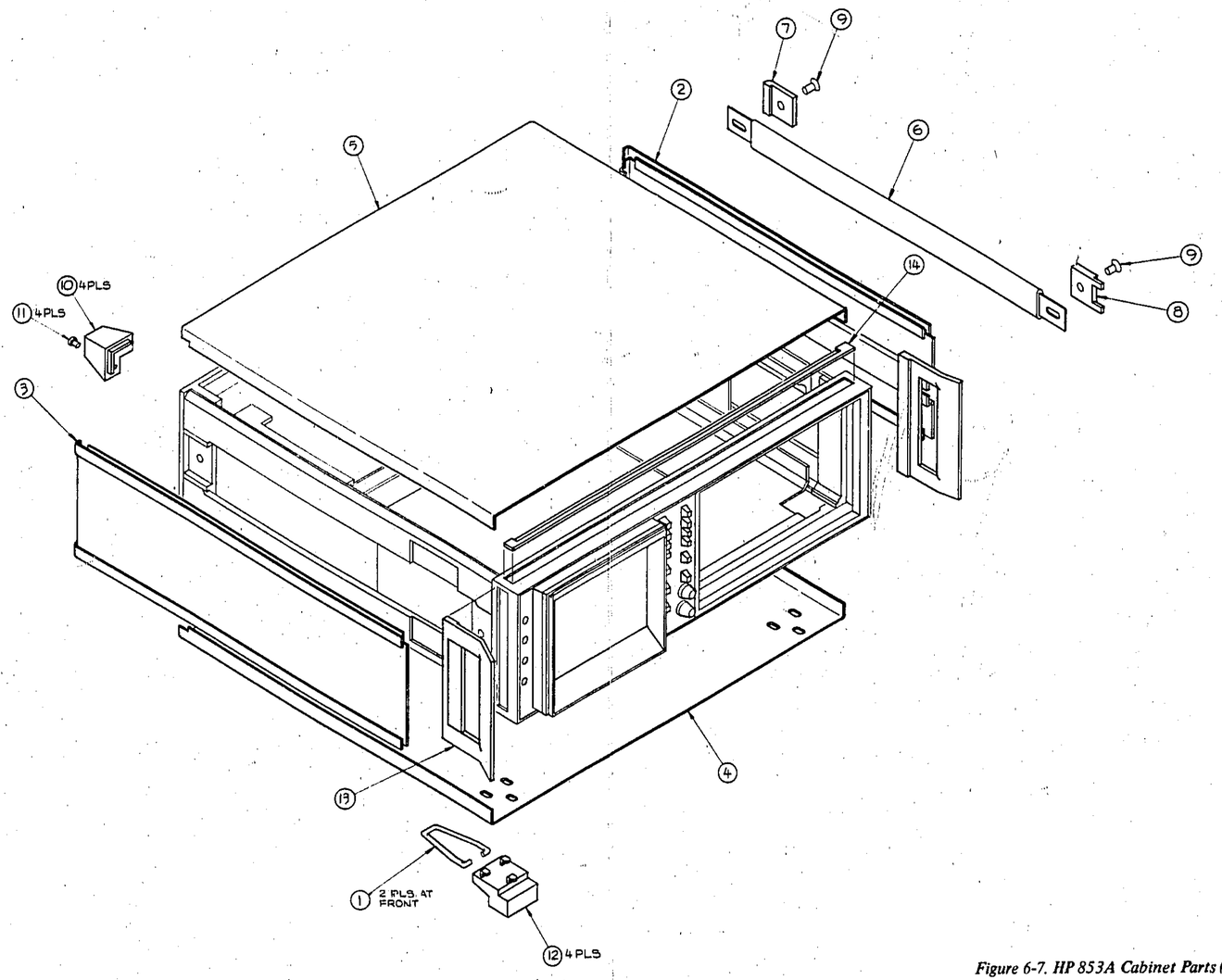


Figure 6-7. HP 853A Cabinet Parts (Option 001)

BACK DATING MANUAL CHANGES

SECTION VII
MANUAL BACKDATING CHANGES

7-1. INTRODUCTION

7-2. This manual applies directly to HP 853A Spectrum Analyzer Displays with the serial number prefix shown under SERIAL NUMBERS on its title page. As time passes, an HP instrument manual might be revised to reflect design changes incorporated into the instrument. In that event, information is provided in this section which enables the user of an older instrument (i.e., one with a serial number prefix lower than the the serial number prefix shown on the revised manual's title page) to change the revised manual so that it pertains to his instrument. Because the HP 853A is a new instrument, no such change information is required in this manual. For additional information about the applicability of the manual relative to the instrument serial number, refer to the paragraph headed INSTRUMENTS COVERED BY MANUAL in Section I.

SERVICE INFORMATION

SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section provides instructions for troubleshooting and repairing the HP 853A Display mainframe. It includes general troubleshooting information, block diagrams of the instrument, circuit descriptions, parts identification illustrations, and schematic diagrams.

WARNING

Troubleshooting and repair of this instrument are performed with power applied to the instrument and protective covers removed. Instrument service should be performed only by service-trained personnel who are aware of the hazards involved. Where maintenance can be performed without power applied, the power should be removed. When any repair is completed, be sure that all safety features, including protective grounds, are intact and functioning.

WARNING

With the ac power cable connected, the ac line voltage is present at the terminals of Primary Switching Assembly A11, Line Filter FL1 (mounted on the rear panel) and at the LINE switch, whether the LINE switch is on or off. When the covers are removed, care must be taken to avoid contact with these exposed terminals, which have voltages capable of causing death. Any maintenance or repair of the opened instrument under voltage should be carried out only by a skilled person who is aware of the hazard involved.

After disconnecting the ac line power cord, allow at least 30 seconds for high-voltage capacitors to discharge before proceeding with maintenance.

8-3. SERVICE INFORMATION INDEX

8-4. Table 8-1 lists specific kinds of information about the spectrum analyzer main assemblies, and indicates where the information is located. The service information for each assembly normally includes a description of the assembly circuits, a diagram showing the locations of the assembly components, and a schematic of the assembly circuits. Service in-

Table 8-1. Service Information Cross-Reference

Assembly Number	Assembly Name	Schematic	Component Location
A1A1	Display Control Assembly	Figure 8-8	Figure 8-6
A2	Display Adjust Assembly	Figure 8-8	Figure 8-7
A3	Display Power Supply Assembly	Figure 8-12	Figure 8-10
A4	High-Voltage Power Supply Assembly	Figure 8-14	Figure 8-13
A5	Data Converter Assembly	Figure 8-26	Figure 8-25
A6	XYZ Amplifier Assembly	Figure 8-34	Figure 8-33
A7	Processor Assembly	Figure 8-43	Figure 8-42
A8	Plug-In Power Supply Assembly	Figure 8-12	Figure 8-11
A9	Interface Assembly	Figure 8-46	Figure 8-45
A10	HP-IB Interconnect Assembly	Figure 8-48	Figure 8-47
A11	Primary Switching Assembly	Figure 8-12	Figure 8-11
A12	Motherboard Assembly	Figure 8-50	Figure 8-49
A13	Fan Module Assembly	Figure 8-12	–
A14	CRT Assembly	Figure 8-14	–

formation for the Processor Assembly, A7, also includes signature analysis troubleshooting information. The circuit descriptions and component locations diagram precede the assembly schematic. The assembly numbers are printed in large, boldfaced, alpha-numeric characters (e.g., A4) in the lower right-hand corner of each schematic diagram.

8-5. SCHEMATIC SYMBOLS, TERMINOLOGY, AND VOLTAGE LEVELS

8-6. Mnemonics for control lines and signal paths are explained on the schematics where they are used. Mnemonics indicating functions of digital components are listed in Table 8-2. Unless indicated otherwise in schematic notes, test conditions for the signal and dc voltage levels shown on the block and schematic diagrams are provided in Table 8-3. Voltage levels are indicated in volts.

8-7. TEST EQUIPMENT

8-8. Test instruments and accessories used to maintain the spectrum analyzer are listed in Table 1-3. If the listed instrument is not available, another instrument that meets the required minimum specifications may be substituted.

Table 8-2. Mnemonics for Digital Component Functions

Mnemonic	Definition	Mnemonic	Definition
CLK IN	clock in	L WR	low write
CLK OUT	clock out	LD	load
CLR	clear	MUX	multiplexer
CNT EN	count enable	R	reset
CNTR	counter	RA	read A
CRY	carry	RB	read B
D	data	RDY	ready
DAC	digital to analog converter	R/W	read/low-write
DIR	direction	S	set
EN	enable	SEL B	select B
ENR	enable read	SER IN	serial in
ENW	enable write	SH/LD	shift/low-load
FF	flip-flop	S.O.	set overflow
INH	inhibit shift	SREG	shift register
L CS	low chip select	U/D	up/down
L EN	low enable	V_{REF}	voltage reference
L IRQ	low interrupt request	WA	write A
L NMI	low non-maskable interrupt	WB	write B
L RD	low read	3-ST	3-state output

Table 8-3. Front-Panel Control Settings for Schematic Measurement Conditions

Function	Setting
853A Display Mainframe	
SCALE INTEN	mid range
TRACE A	CLEAR WRITE
TRACE B	CLEAR WRITE
INTEN	mid range
All other settings	OFF
Plug-In	
INPUT ATTEN (dB)	10 dB
Amplitude Scale	10 dB/DIV
FREQ SPAN/DIV	INTERFACE ASSEMBLY A9: 5 MHz ALL OTHER ASSEMBLIES: 10 MHz
RESOLUTION BW	1 MHz
TIME/DIV	AUTO
TRIGGER	FREE RUN
START–CENTER	CENTER
BASELINE CLIPPER	OFF
VIDEO FILTER	OFF
TUNING	Center CAL OUTPUT signal.
REFERENCE LEVEL REF LEVEL FINE	Set CAL OUTPUT signal peak at REFERENCE LEVEL.

TROUBLESHOOTING – GENERAL

General Troubleshooting Procedure

The following procedure isolates a failure to the assembly level.

1. After checking the line voltage selector and line fuse F1 located on the instrument rear panel, turn the HP 853A LINE switch on. The instrument should complete a self-check within 5 seconds. The self-check tests System Memory, Stroke Memory, and program memory (ROM) on Processor Assembly A7, using digital storage test routines #7, #8, and #9. If the self-check fails because of memory failure, the CRT displays one or two indicators that locate the faulty memory component(s). Table 5-5 defines the indicators. Test routines are described in Section V.

2. To check analog circuitry, bypass the digital circuitry by pressing both STORE BLANK push buttons. In analog display mode, the HP 853A functions as a conventional CRT display. Check for a normal analog CRT trace while varying front panel controls. If the STORE BLANK push buttons fail to activate analog display mode, Processor Assembly A7 might have a circuit failure. Verify this by disconnecting Processor Assembly A7 from the HP 853A. The mainframe automatically defaults to analog display mode when the digital control circuitry is removed.

   Proper operation of the HP 853A during analog display mode verifies that the power supplies (A8, A3, A4), CRT, deflection amplifiers (A6), and sections of the interface circuitry (A7) are operational. Proceed to troubleshoot these circuits as necessary if problems are apparent.

3. If the HP 853A functions normally in analog display mode, most circuit problems are located on Data Converter Assembly A5, Processor Assembly A7, or Interface Assembly A9.

Test routines, described in detail in Section V, exercise the mainframe digital circuitry. Instructions for all test routines are contained in the Program ROM, A7U34. To activate the test routines, switch LINE power off, then on, with the PLOT GRAT push button depressed. Successive pressing of the PLOT GRAT push button selects all of the test routines. The test routines cannot be accessed when the mainframe is in analog display mode.

4. Problems in the digital storage output circuitry located on Data Converter Assembly A5 can be confirmed using digital storage test routines #0, #1, #3 and #4. The CRT patterns for these test routines are generated without using the digital storage input circuitry. During these test routines, digitized sweep and video information from the plug-in is not stored in Stroke Memory and System Memory. Instead, the CPU stores programmed digital information. The Data Converter Assembly, A5, converts this into analog signals which are processed by the XYZ Amplifier Assembly, A6, and displayed on the CRT. Figure 5-3 shows the stroke generator test pattern generated by test routine #1.

5. If test routine #1 indicates that the digital storage output circuitry is functioning properly, proceed to check the digital storage input circuitry by selecting digital storage test routine #5. The PLOT TRACE push button can then be pressed to manually select the input signal to Data Converter Assembly A5 (P1-50). Data values stored in memory are displayed on the CRT to aid in troubleshooting. Figure 5-5 shows a typical CRT display for test routine #5.

   If test routine #5 indicates a possible problem in the maximum peak detector circuitry, perform the peak detector droop test in the Digital Storage Adjustments (paragraph 5-14) using test routine #2.

6. The Processor Assembly, A7, contains most of the digital circuitry in the HP 853A. Use the signature analysis troubleshooting procedure detailed in Figure 8-41 to troubleshoot this assembly. The procedure detects a high percentage of digital failures.

7. Perform the Operation Verification procedure as outlined in Section V to verify proper operation of the HP 853A with an RF plug-in.

TROUBLESHOOTING – SIGNATURE ANALYSIS

Signature analysis troubleshooting information for Processor Assembly A7 is provided in Figure 8-41. Use HP Model 5004A or HP Model 5005A Signature Analyzer.

Figure 8-1 describes how to use the signature analysis troubleshooting diagrams.

Use of Signature Analysis Troubleshooting Diagrams

1. Connect signature analyzer and set controls according to diagram instructions.

2. Set up test configuration as indicated (connect and/or remove special test jumpers, etc.).

3. Verify the +5 Vdc signature for the test being performed, as indicated in green lettering on main verification path (green line). This signature can be verified by probing the +5 Vdc supply or by pushing and releasing the reset key on the signature analyzer probe. If +5 Vdc signature is incorrect, first check equipment settings and connection. Then check for activity at CLOCK, START, and STOP connections using signature analyzer probe. If no activity, refer to appropriate schematic for troubleshooting.

4. Begin probing the printed circuit board at the beginning of the green line on the diagram (A).

5. Probe every point indicated by the green line.

6. If signature at node is incorrect, node is suspect. Information printed in red on the troubleshooting diagram is helpful for tracing problem to its source; location instructions (B) indicate the next closest pin connected to the circuit node. For example, instruction "24-5" indicates that a circuit node signature originates at U24, pin 5. (Note that pin 1 on each IC is square.)

   Interconnecting red lines show related input and output pins. Red lines (C) connect inputs that affect only the outputs to which they are connected.

   Interconnecting black lines (D) represent a physical connection between IC pins.

7. To locate the faulty source node, use the troubleshooting diagram and circuit schematics to check signatures.

8. Verify signatures to all IC pins connected to a suspect node. If all signatures for a circuit node are not identical, the printed circuit board, connectors, and solder joints should be checked for faults. After locating faulty node, proceed with conventional troubleshooting. Use the HP 546A Logic Pulser and HP 547A Current Tracer.

9. Before replacing any suspected defective component, follow instructions printed in red on the troubleshooting diagram. These troubleshooting instructions are usually referenced by an asterisk (*).

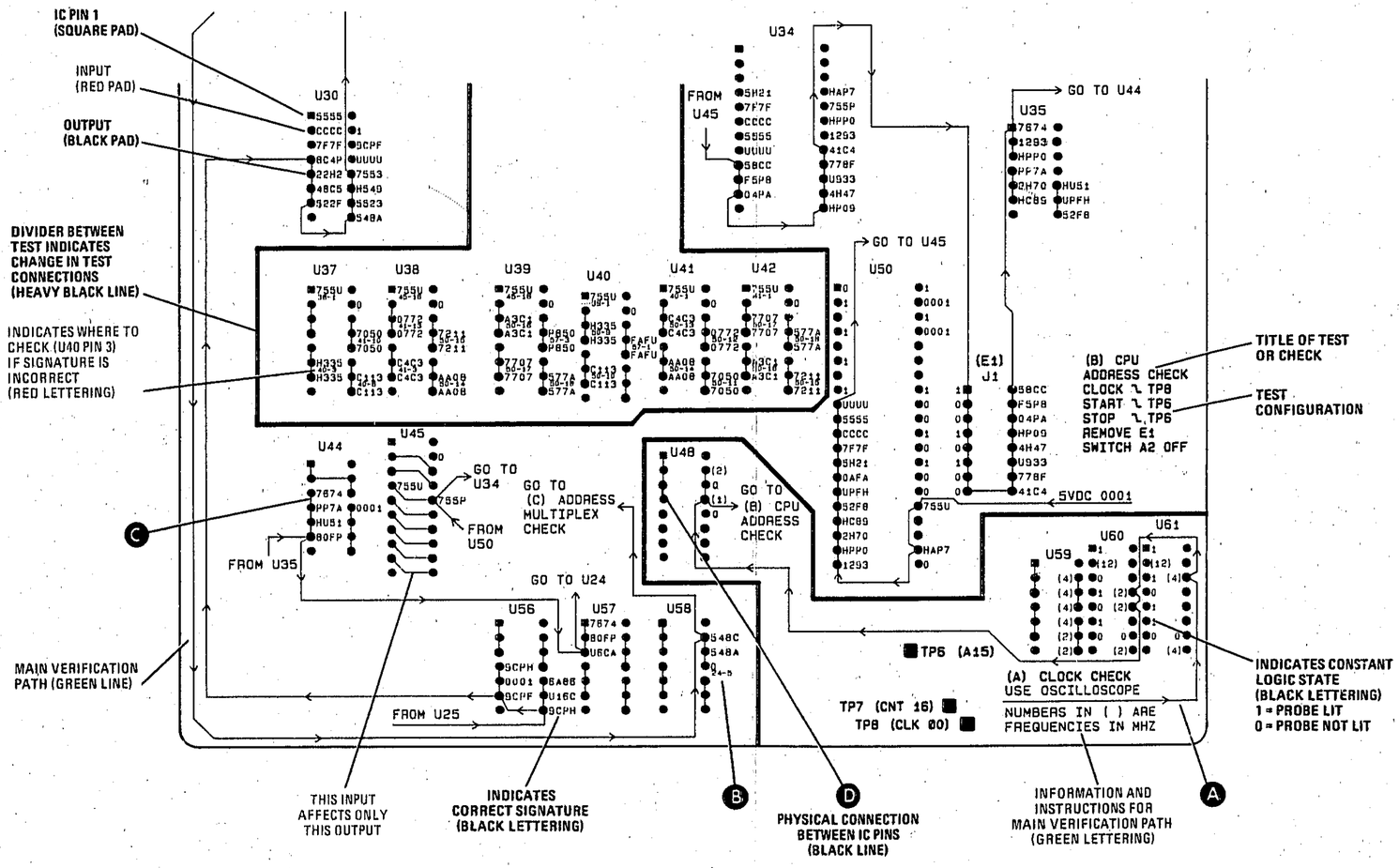


Figure 8-1. General Signature Analysis Troubleshooting Instructions

GENERAL CIRCUIT DESCRIPTION

The HP 853A consists of two major functional systems called the Input System and the Output System. Figures 8-4 and 8-5 are functional block diagrams, showing analog and digital signal flow. The Input System is shown on the left side and the Output System is on the right side of Figure 8-5.

The Input and the Output Systems function asynchronously and independently. The central processing unit (CPU) controls the Input System. The Counter controls the Output System. (See Figure 8-2.) The Input System measures VIDEO and SWEEP information generated by the plug-in, converts it to digital data and stores it in Stroke Memory. The Input System also collects information from various interfaces and latches, and stores this information in Stroke or System Memory. Data corresponding to front panel control settings is stored in System Memory. The Output System fetches data from System and Stroke Memory and displays it on the CRT as traces, graticules, and characters.

The Input System is a microcomputer. In the HP 853A, the microcomputer is part of the Processor Assembly, A7. Refer to Figure 8-3.

The CPU performs arithmetic and logic operations. It contains enough memory to provide temporary storage for its internal operation.

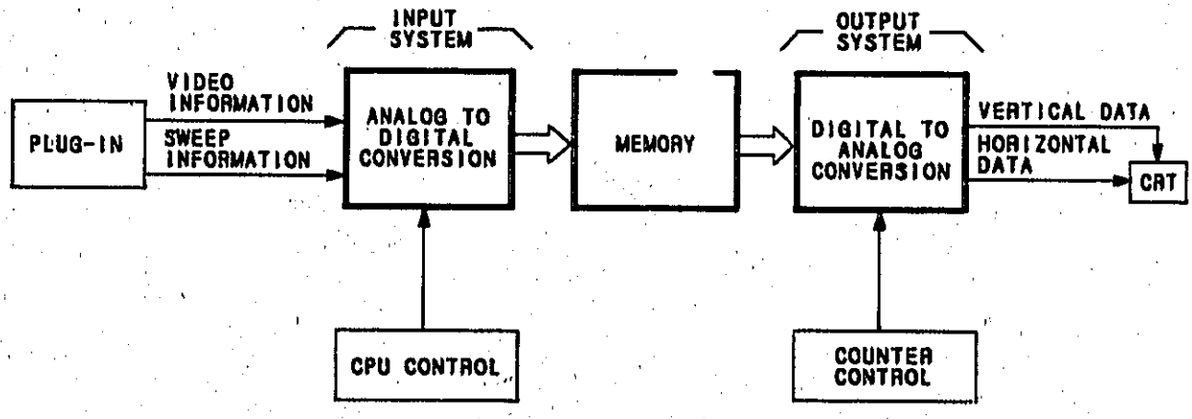


Figure 8-2. CPU and Counter Control the Input and Output Systems

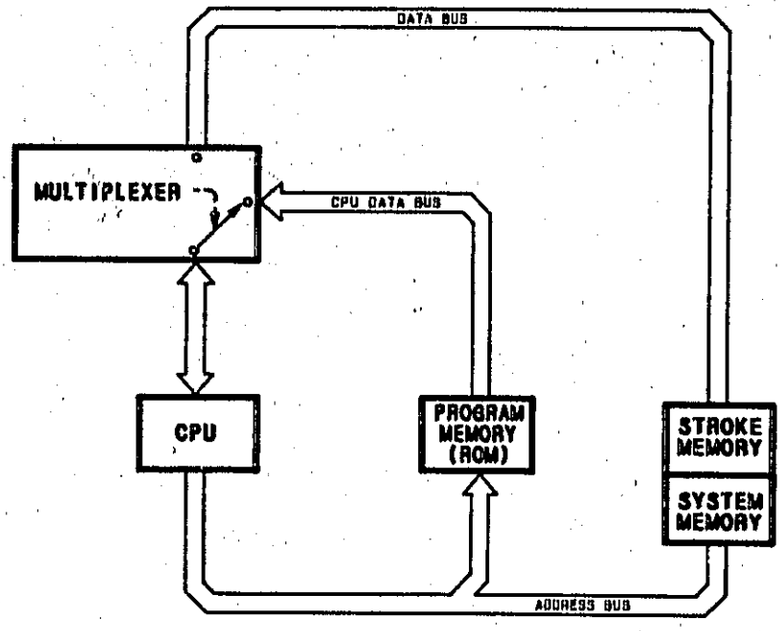


Figure 8-3. Microcomputer Block Diagram

The Program ROM is memory that contains instructions for the CPU. These instructions are communicated to the CPU via the CPU Data Bus.

Stroke and System Memories contain data arranged by address.

The CPU manipulates data that it fetches from certain addresses in Stroke or System Memory, according to instructions that it receives from the Program ROM. The CPU stores its calculations in Stroke and System Memory.

The Program ROM also receives signals from the CPU. These signals may determine the next-step instructions that the CPU will execute.

The CPU measures the analog SWEEP voltage (−5V to +5V) and the analog VIDEO signal. The CPU uses the Control Latches in Processor Assembly A7 to control the circuitry in Data Converter Assembly A5 that converts the analog signals to digital information. This circuitry consists of Multiplexer, Peak Detectors, Track and Hold, and Analog to Digital Converter. During normal operation, the CPU alternately takes samples of the horizontal and vertical signals; the value of the SWEEP signal (X) determines the memory address at which the VIDEO (Y) value is stored.

The Counter in the Processor Assembly A7 controls the other major function of the HP 853A; it fetches stroke and character data from Stroke and System Memory and converts it to individual strokes which are displayed on the CRT.

The Counter controls the Output System via the Counter and Data Busses. The Counter uses the data bus only when the CPU is accessing an instruction from the Program ROM via the CPU Data Bus. Thus, the CPU and the Counter use the same data bus, but not at the same time.

The Counter accesses Stroke Memory for trace data. The CPU (Input System) has processed the VIDEO signal (Y) and has sequentially stored stroke data in Stroke Memory at 512 addresses. The addresses correspond to 512 horizontal positions on the CRT. The vertical axis of the CRT is divided into 800 values. The stroke data stored corresponds to the y value of the VIDEO signal at each of these horizontal positions. The Counter samples the stroke data at these 512 addresses sequentially and routes it through the Y Data Buffer to the Digital Y Generator, located in the Data Converter Assembly, A5. The Digital Y Generator and the Y Amplifier (A6) process the stroke data to provide 512 vertical deflection signals for the CRT, which correspond to the 512 horizontal positions. This process produces a trace consisting of 512 individual strokes.

Data Converter Assembly A5 generates a horizontal deflection signal (DGTL X) used during digital display mode. The Digital X Generator in A5 receives control signals from the Counter in A7 and generates a ramp that is amplified in the XYZ Amplifier Assembly, A6, and passes to horizontal deflection plates of the CRT.

The intensity and focus of each stroke is modulated. The Z-axis signal (CONTROL GATE), generated in XYZ Amplifier Assembly A6, controls both the brightness and the blanking of the trace. The Digital Y Generator in Data Converter Assembly A5 sends stroke length information to the Control Gate Amplifier in A6. Stroke length information modulates the stroke intensity so that long and short strokes have similar intensity. Information corresponding to the horizontal position of the trace modulates stroke focus in the Focus Gate Amplifier in A6. Blanking Logic in Processor Assembly A7 combines all blanking inputs and control logic inputs to produce one blanking signal for the CRT.

The Counter displays dot matrix characters on a raster by modulating the intensity of a series of ramps. The Character Generator on Processor Assembly A7 converts ASCII code (American Standard Code for Information Interchange) to blanking information which is processed by Blanking Logic in A7, and amplified by the Control Gate Amplifier in A6 to modulate the Z-axis of the CRT. The ramps are formed by loading two values into the Y Data Buffer (A5), which are then alternately loaded into the Digital Y Generator. The Digital Y Generator draws strokes between these two values to form the raster.

Graticule illumination is also formed by a series of ramps. Values corresponding to zero and full-scale CRT beam deflection are loaded into the Y Data Buffer on Data Converter Assembly A5. These values are then alternately loaded into the Digital Y Generator which draws strokes between them to form 512 full-scale ramps. The CRT beam is defocused to give uniform illumination.

All information that passes between the plug-in and the HP 853A Display mainframe passes through the Interface Assembly, A9.

The CPU monitors various interfaces and latches. They communicate front panel control settings, sweep status signals from the plug-in, HP-IB address code, and HP-IB Input/Output signals.

During digital display mode, the Counter refreshes the display every 17.9 ms. At sweep speeds slower than 5 msec/DIV, the CPU stores SWEEP and VIDEO information at the same rate as the plug-in sweep.

At sweep speeds of 5 msec/DIV or faster (10 msec/DIV or faster when using digital average mode), the CPU does not have enough time to process the SWEEP and VIDEO signals to digital information. To maintain display information, analog traces and digitally controlled character and graticule information are displayed alternately on the CRT. This is called mixed mode. The Comparator in Interface Assembly A9 monitors plug-in sweep speeds and signals when sweep speeds are greater than or equal to 5 msec/DIV (or 10 msec/DIV). The Counter and Blanking Logic in A7, and the Comparator in A9 interact, producing a signal which steers digital or analog information through the Digital/Analog Switch in the XYZ Amplifier Assembly, A6. (For detailed description of mixed mode, refer to Counter section of Processor Assembly A7 circuit description.)

When the mainframe is in analog mode (press front panel controls STORE BLANK), the VIDEO and SWEEP signals from the plug-in are routed directly to the XYZ Amplifier Assembly A6, at pin 50. Thus, in analog mode, VIDEO and SWEEP bypass the digital circuitry and are displayed as analog traces on the CRT.

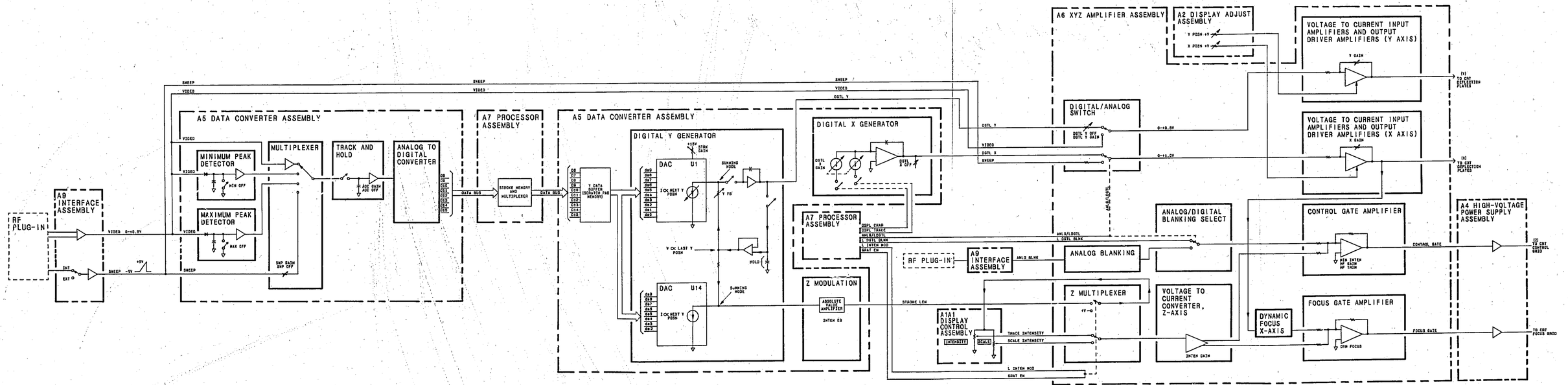


FIGURE 8-4. ANALOG SIGNAL FLOW, BLOCK DIAGRAM

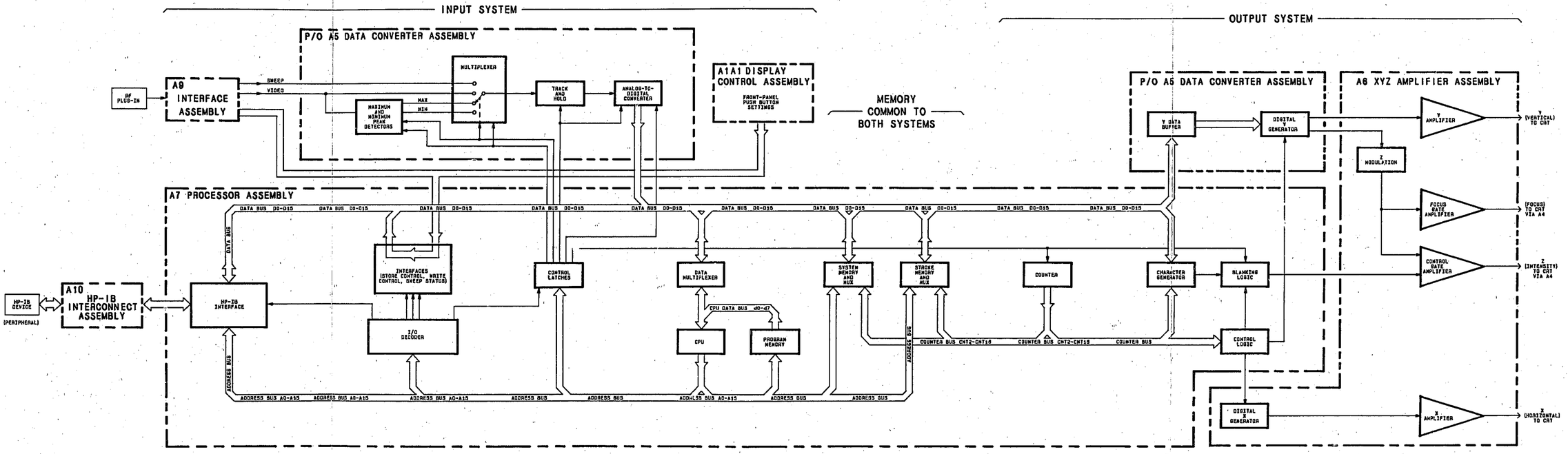


FIGURE 8-5. DIGITAL SIGNAL FLOW, BLOCK DIAGRAM

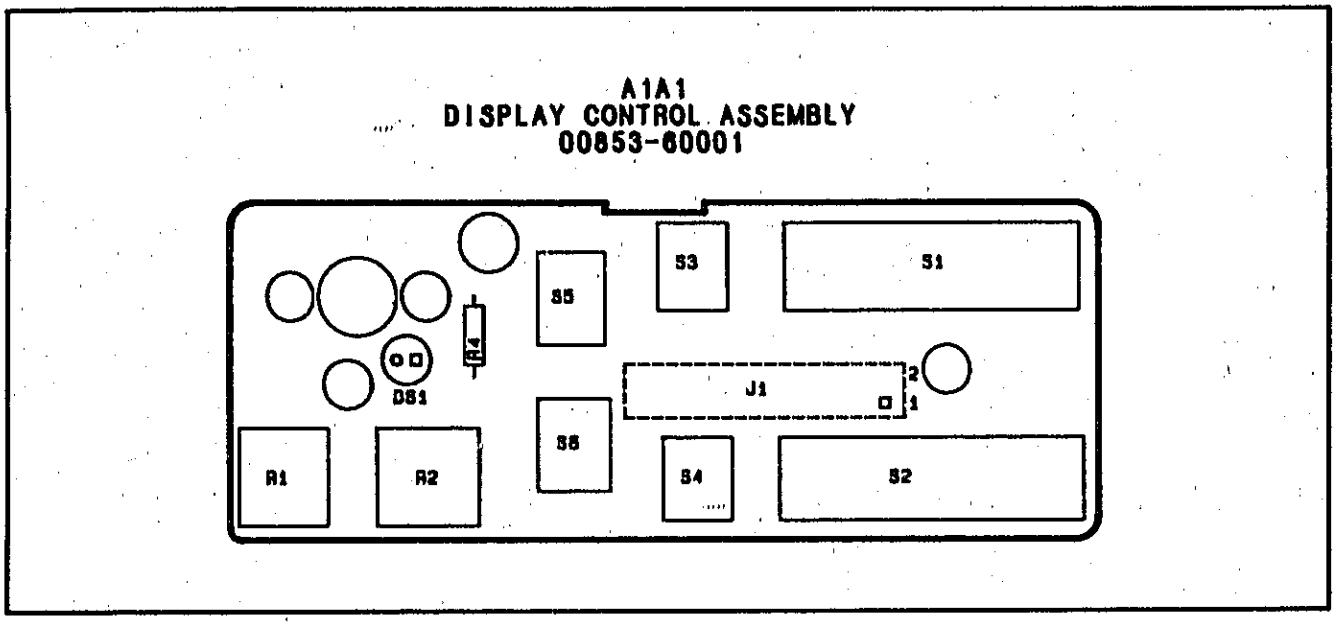


Figure 8-6. Display Control Assembly A1A1, Component Locations

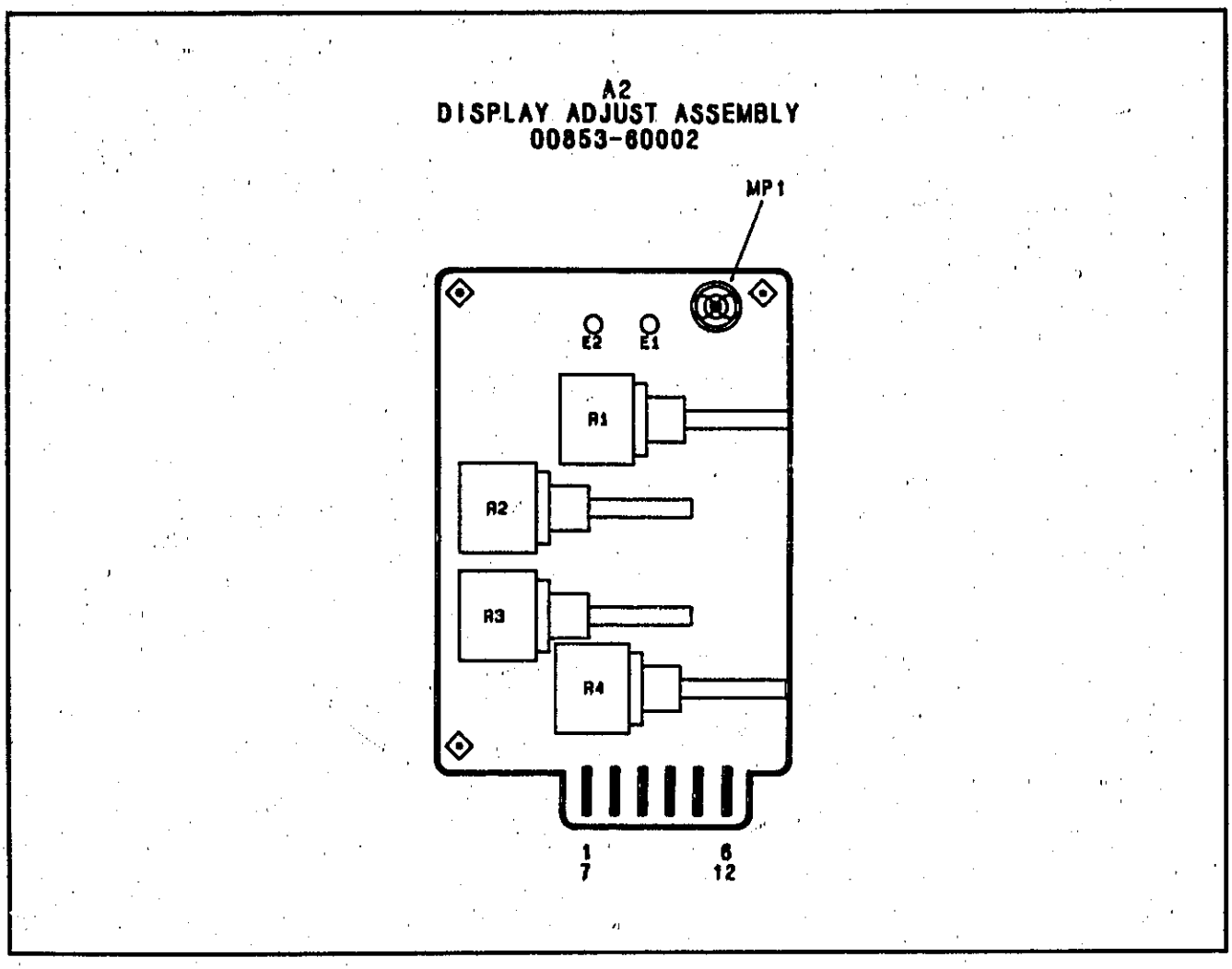


Figure 8-7. Display Adjust Assembly A2, Component Locations

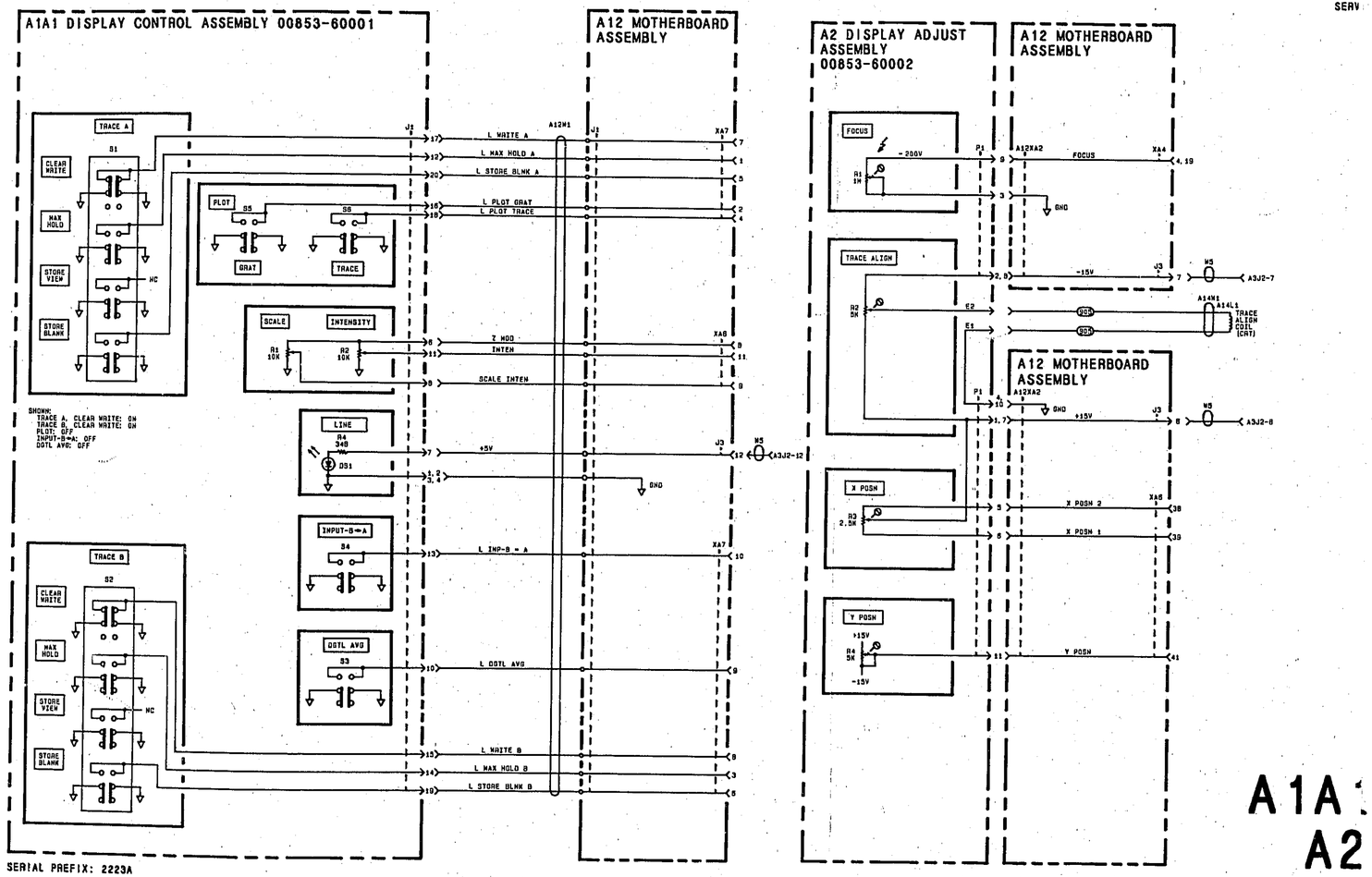


FIGURE 8-8. DISPLAY CONTROL ASSEMBLY A1A1 AND DISPLAY ADJUST ASSEMBLY A2, SCHEMATIC DIAGRA

8-15/8-1

A1A1
A2

PRIMARY SWITCHING ASSEMBLY A11, PLUG-IN POWER SUPPLY ASSEMBLY A8, DISPLAY POWER SUPPLY ASSEMBLY A3, AND FAN MODULE ASSEMBLY A13, CIRCUIT DESCRIPTION

Primary Switching Assembly A11, Plug-In Power Supply Assembly A8, and Display Power Suppiy Assembly A3 produce the low-voltage power supplies.

Primary Switching Assembly A11 connects transformer T1 windings according to the settings of A11S1 and A11S2.

The voltages from three of the transformer secondary windings pass to Plug-In Power Supply Assembly A8, where they are rectified to three unregulated dc voltages. The unregulated voltages are regulated on assembly A8 to +15V (PLUG-IN), +100V, and −12.6V, and drive the plug-in. The unregulated voltages also pass to Display Power Supply Assembly A3, where they are regulated to +15V, −15V, and +158V, and drive the HP 853A Display mainframe. Assembly A3 also produces a regulated dc voltage that drives the Fan Module, A13.

The voltage from the fourth transformer secondary winding passes to Display Power Supply Assembly A3, where it is converted to an unregulated dc voltage and regulated to +5V to drive the mainframe.

The +100V supply is disabled when the plug-in is not installed.

PRIMARY SWITCHING ASSEMBLY A11

The two primary windings of transformer T1 can be connected in four different series or parallel combinations by switches S1 and S2. Figure 8-9 shows the transformer primary connections for line voltages of 100 Vac, 120 Vac, 220 Vac, and 240 Vac.

Thermal switch S1 senses the temperature at the rear panel, and opens at temperatures exceeding 90°C, turning off primary power.

PLUG-IN POWER SUPPLY ASSEMBLY A8

+200V Rectifier A

Diodes CR1 through CR4 and filter capacitor C2 are connected as a full-wave bridge rectifier which produces an unregulated dc voltage of approximately +200V. Radio frequency interference (RFI) is reduced by C1.

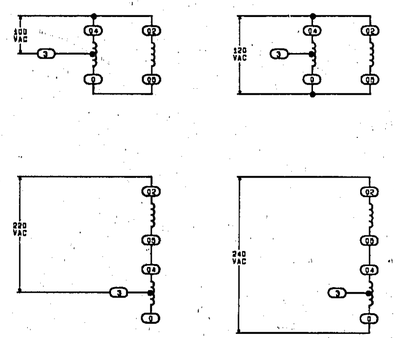


Figure 8-9. Transformer Primary Connection for Selected Line Voltage

+26V Rectifier ⓑ

Diodes CR9 and CR10 and filter capacitor C5 are connected as a full-wave, center-tapped rectifier which produces an unregulated dc voltage of approximately +26V. Capacitors C13 and C14 filter RFI.

A crowbar circuit reacts to primary power overvoltage. When the line input voltage exceeds the selected value by approximately 40%, the +26V Rectifier output exceeds the breakdown voltage of zener diode VR3, producing positive voltage at the gate of SCR Q5. When Q5 conducts, a large primary current in transformer T1 blows fuse F1. Resistor R21 maintains zero gate voltage unless the breakdown voltage of VR3 is exceeded.

−24V Rectifier ⓒ

Diodes CR14 and CR15 and filter capacitor C9 are connected as a full-wave, center tapped rectifier which produces an unregulated dc voltage of approximately −24V. Capacitors C15 and C16 reduce conducted RFI. Resistor R11 provides an isolated ac output to the plug-in, for line-triggered sweep.

+100V Regulator ⓓ

Transistors Q1, Q2, and Q4 form a feedback amplifier that converts the unregulated voltage from the +200V Rectifier to a regulated +100V supply for the plug-in (25 mA maximum). Transistor Q2 is the driver for Q4. The emitter of Q1 is connected through CR8 to the +15V supply, which serves as reference. The +100V output is divided by R6 and R7, and compared to the +15V reference at the base of Q1.

Feedback action is as follows. If the output is higher than +100V, the base-emitter voltage of Q1 is high, causing more collector current to flow in Q1. This decreases the base current to Q2, and thus lowers the voltage at the base of Q2. Since Q2 and Q4 are connected as series emitter followers, the emitter voltage of Q4 decreases to maintain a stable +100V output.

Feedback loop stability is provided by C3. Resistor R8 provides bias current for CR8. Diode CR6 prevents excessive current through Q1 when the supply output is shorted to ground. Diode CR7 protects Q1 from reverse bias. Power dissipation in Q4 is reduced by R1. Overvoltage protection is provided by F3 and VR4.

Transistor Q3 is normally off, and provides current limiting at about 32 mA. The emitter of Q3 is connected to the supply output, which is normally independent of load current. As the load current increases, the voltage across R3 also increases. This increases the voltage at the base of Q4, and at the base of Q3 through divider network R4 and R5. When the load current increases to about 32 mA, Q3 turns on. The voltage at the base of Q2, and the output voltage decreases. This circuit is a foldback current limiter which has less current at short circuit than at its maximum current capabilty.

When a plug-in is not installed, Q6 turns off the +100V supply. Current flowing through R2 passes through R20 to ground, decreasing voltage at the base of Q2; the output voltage decreases to less than +20V. When a plug-in is installed, the base of Q6 is grounded, turning Q6 off and enabling the +100V supply. The supply can also be enabled by grounding TP3 (ENABLE).

+15V Regulator ⓔ

Voltage regulator U1 supplies +15.05V to the plug-in. It maintains a +1.25V reference voltage between the OUT and ADJ terminals. This voltage is applied across R14, producing a current which flows through R12 and R13. The voltage at the ADJ terminal is determined by the voltage drop across R12, and R13 plus the breakdown voltage of VR1. The output voltage is 1.25V greater than the ADJ terminal voltage.

Capacitor C7 provides noise filtering. Diode CR12 discharges C7 and protects U1 when the output is grounded; CR11 protects U1 if the input is grounded. Resistor R15 provides bias to LED DS2 when the supply is on. Diode CR13 provides reverse-voltage protection.

When overvoltage occurs, a zener diode in the plug-in causes excess current to blow F1. If the supply output is shorted to ground, F1 usually blows, unless Q1 limits the current to a value lower than the fuse rating.

−12.6V Regulator (F)

Voltage regulator U2 operates similar to U1, and provides −12.65V to the plug-in. Resistor R23 reduces the power dissipation of U2. When the output is grounded, F2 usually does not blow. (U2 contains current limiting circuitry.)

DISPLAY POWER SUPPLY ASSEMBLY A3

+158V Regulator (G)

Operation is similar to the +100V Regulator, except that a constant current source provides base current for Q2. Zener diode VR1 is biased to about 2.5V by R5, which produces a drop across R1, causing 0.6 mA to flow in Q3. Divider network R6 and R7, and R2 set the current limit.

+15V Regulator (I)

Voltage regulator U1 is similar to A8U1 and supplies +15V to the mainframe. Overvoltage protection is enabled when the output voltage is high enough to forward bias VR7. This turns on SCR Q7, which shunts the output and causes U1 to current limit.

When cable W5 (connects A3 to motherboard) is disconnected, CR16 and CR17 provide a ground-return path from the unregulated voltages on A8 to the circuits on A3.

−15V Regulator (J)

Voltage regulator U3 is similar to U1 and supplies −15V to the mainframe. Transistor Q8 (SCR) provides overvoltage protection.

+11V Rectifier (K)

Diodes CR12 through CR15 and filter capacitor C12 form a full-wave bridge rectifier that produces an unregulated dc voltage of about +11V. C15 reduces conducted RFI. Fuse F1 blows if any of the rectifier components are shorted. R19 and CR11 provide an alternate ground-return path when W5 is not connected.

+5V Regulator (L)

Voltage regulator U4 is similar to A8U1 and supplies +5V to the mainframe. Overvoltage protection is provided by SCR Q6.

CRT Bias (H)

This circuitry establishes voltages for astigmatism and pattern adjustments, and the accelerator mesh of the CRT.

FAN MODULE ASSEMBLY A13

Fan Regulator (M)

Regulator U2 produces an output voltage of about −12V that drives the Fan Module Assembly, A13. CR4 provides reverse−voltage protection. C6 stabilizes U2.

Fan Module Assembly A13 converts the −12 Vdc input to three ac signals which drive the field coils of the brushless dc fan B1.

Troubleshooting

Each of the regulated supplies has an LED. When one or more of these are unlit, check for a blown fuse in that circuit. If all the LEDs are unlit, check the primary circuit.

Do not short the +100V supply when a plug-in is installed. This causes excess current to flow through the vertical driver of the plug-in, from the +15V Regulator to the grounded +100V line, causing A8F1 to blow.

The +100V supply uses the +15V supply as a reference. Therefore, the +100V supply turns off when the +15V is off.

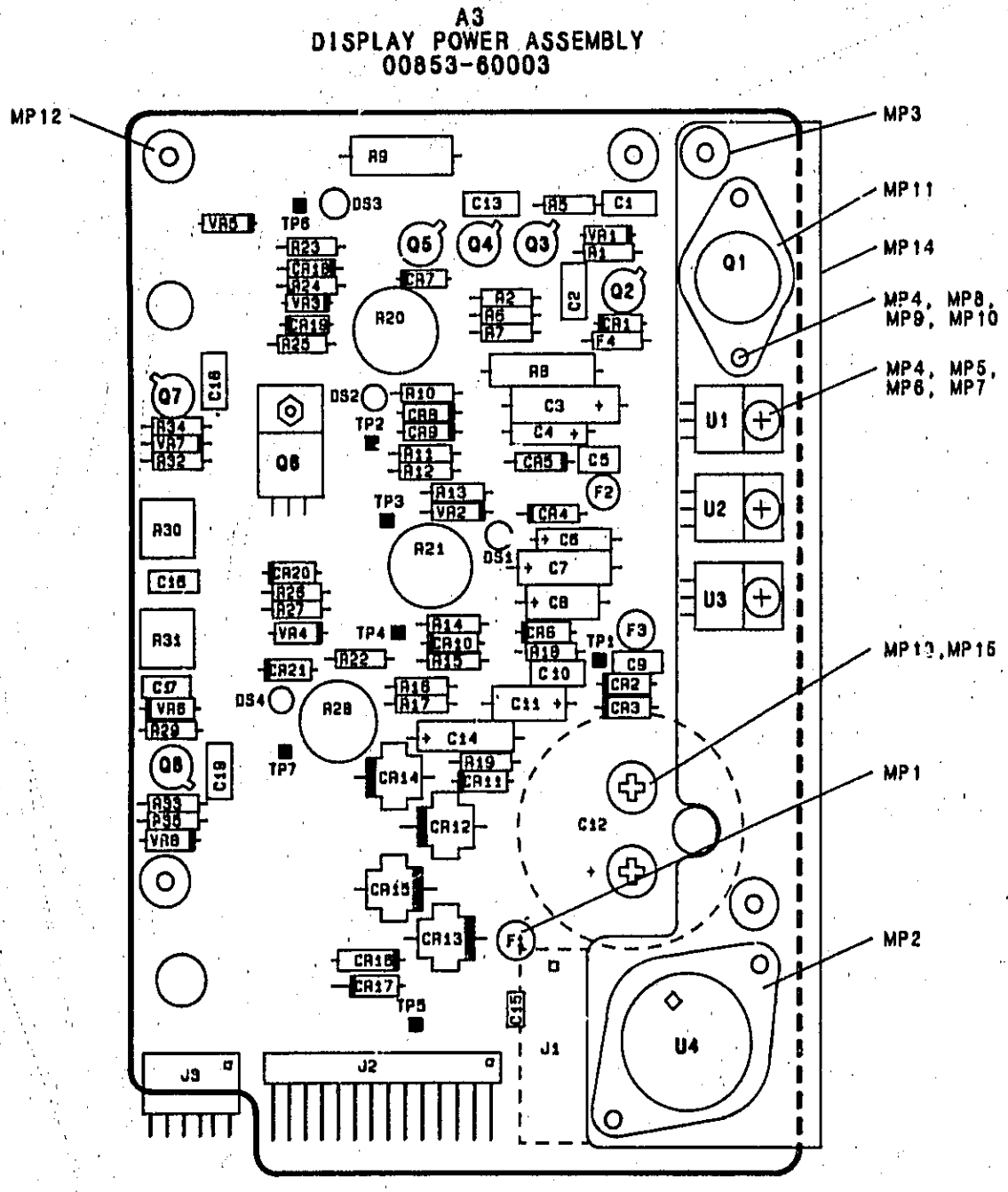


Figure 8-10. Display Power Supply Assembly A3, Component Locations

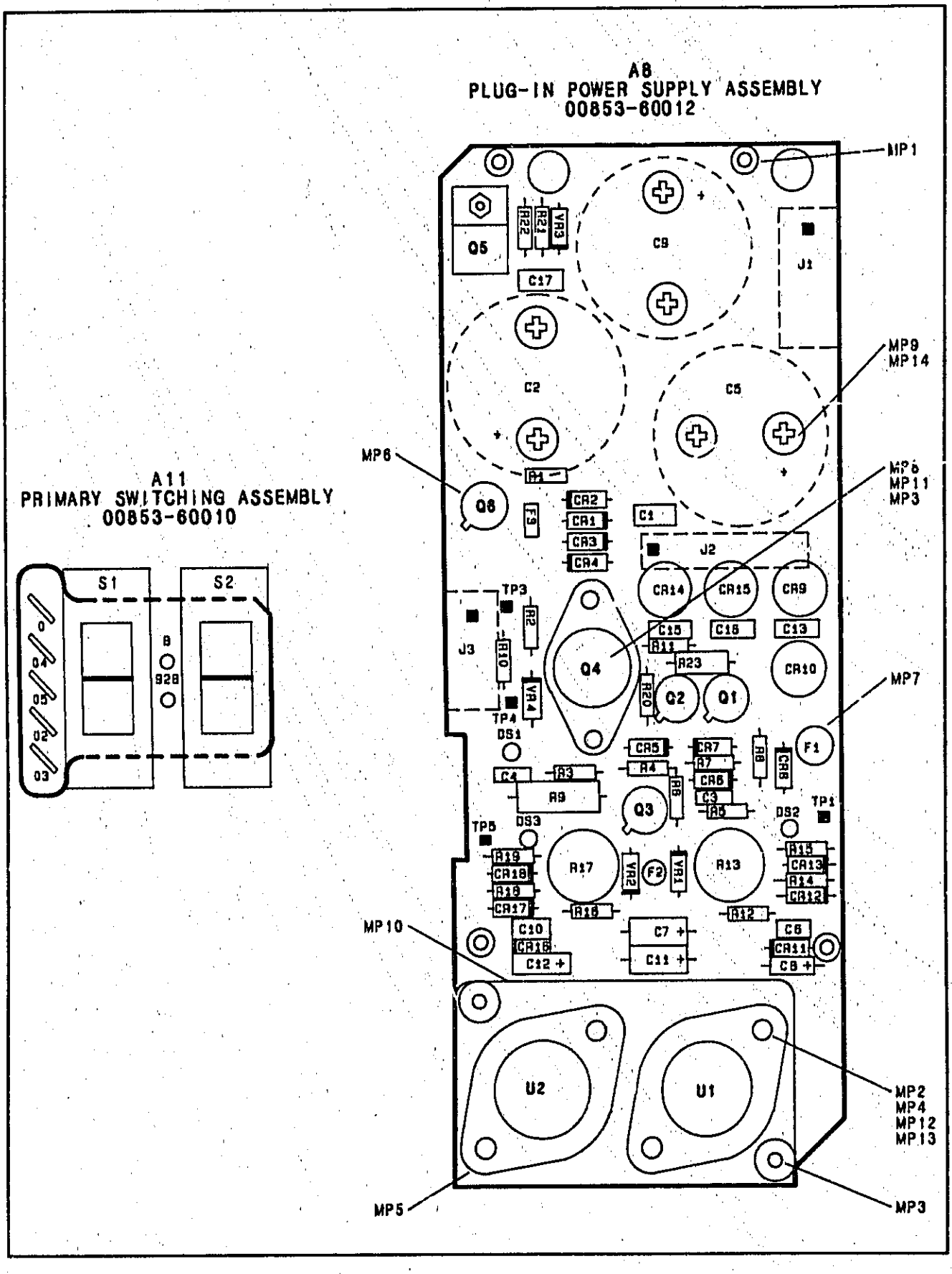


Figure 8-11. Plug-In Power Supply and Primary Switching Assemblies, A8 and A11, Component Locations

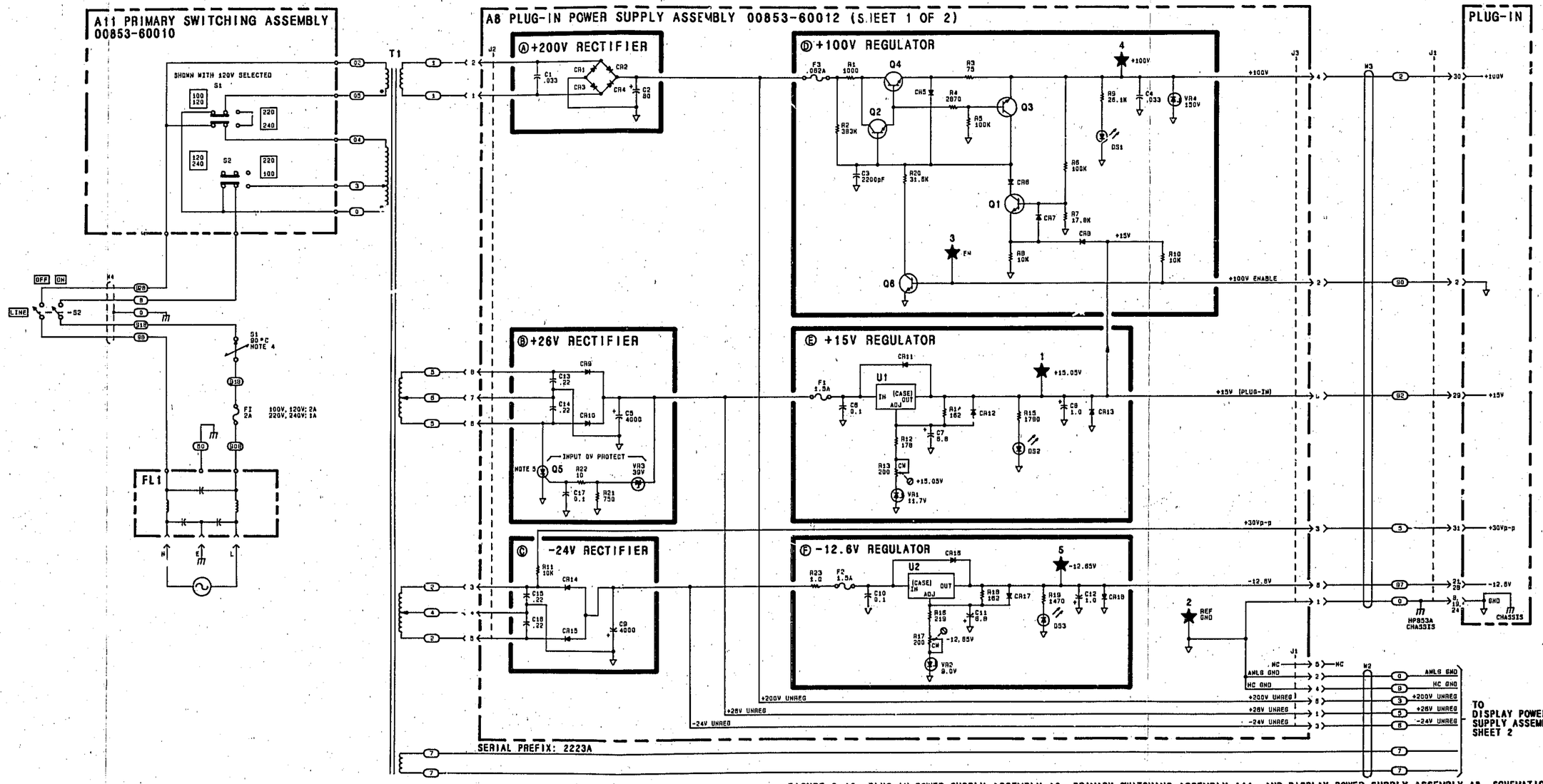
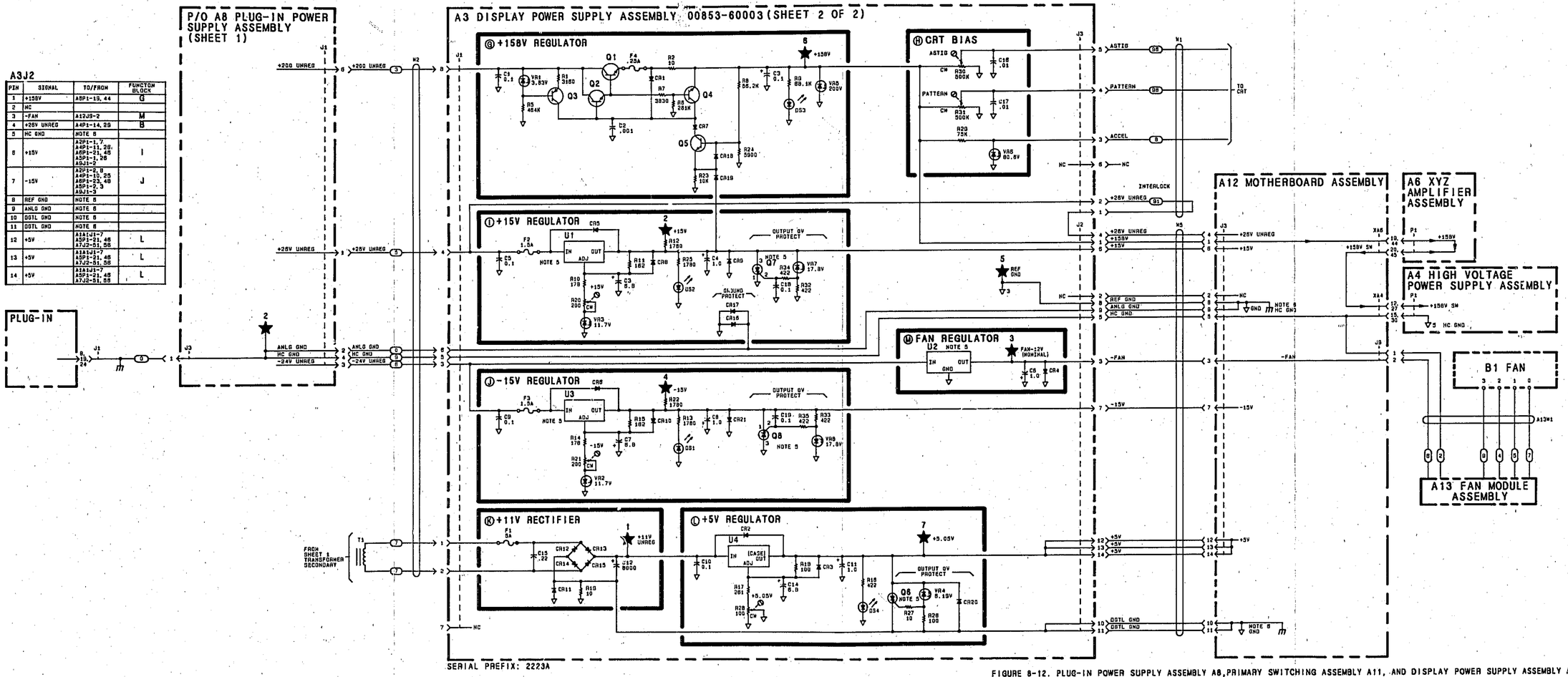


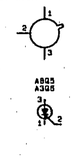
FIGURE 8-12. PLUG-IN POWER SUPPLY ASSEMBLY A8, PRIMARY SWITCHING ASSEMBLY A11, AND DISPLAY POWER SUPPLY ASSEMBLY A3, SCHEMATIC DIAGRAM (1 OF 2)



PIN	SIGNAL	TO/FROM	FUNCTION BLOCK
1	+158V	A8P1-19, 44	G
2	NC		
3	-FAN	A12J9-2	M
4	+26V UNREG	A4P1-14, 29	B
5	HC GND	NOTE 6	
6	+15V	A2P1-1, 7 A4P1-11, 28 A8P1-21, 45 A5P1-1, 26 A9J1-2	I
7	-15V	A2P1-2, 8 A4P1-10, 25 A8P1-23, 48 A5P1-2, 3 A9J1-3	J
8	REF GND	NOTE 6	
9	ANLG GND	NOTE 6	
10	DGTL GND	NOTE 6	
11	DGTL GND	NOTE 6	
12	+5V	A1A1J1-7 A5P1-21, 46 A7J2-51, 56	L
13	+5V	A1A1J1-7 A5P1-21, 46 A7J2-51, 56	L
14	+5V	A1A1J1-7 A5P1-21, 46 A7J2-51, 56	L

NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. FOR COMPLETE REFERENCE DESIGNATION, PREFIX ABBREVIATION WITH ASSEMBLY DESIGNATION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IS IN OHMS (Ω) CAPACITANCE IS IN MICROFARADS (μF) INDUCTANCE IS IN MICROHENRIES (μH)
3. UNLESS OTHERWISE INDICATED, SIGNALS ENTER AT LEFT SIDE AND EXIT AT RIGHT SIDE OF FUNCTION BLOCKS.
4. THERMAL SWITCH OPENS AT TEMPERATURES GREATER THAN 90°C.
5. A8J7, A8J8



6. REF GND, ANLG GND, AND DGTL GND CONNECT TO CHASSIS (GND) AT THE MOTHERBOARD ASSEMBLY A12. DGTL GND CARRIES RETURN CURRENT FOR MOST DIGITAL CIRCUITS. HC GND CARRIES RETURN CURRENT FOR THE H.V. POWER SUPPLY AND FAN. ANLG GND CARRIES RETURN CURRENT FOR MOST OTHER ANALOG CIRCUITS. ALL DISPLAY POWER SUPPLY VOLTAGES ARE REFERENCED TO REF GND.
7. MNEMONIC TABLE:

MNEMONIC	DESCRIPTION
ACCEL	ACCELERATOR MESH
ANLG GND	ANALOG GROUND
ASTIG	ASTIGMATISM
REF GND	REFERENCE GROUND
DGTL GND	DIGITAL GROUND
HC GND	HIGH CURRENT GROUND
UNREG	UNREGULATED
+158V SW	+158V SWITCHED

A3

FIGURE 8-12. PLUG-IN POWER SUPPLY ASSEMBLY A8, PRIMARY SWITCHING ASSEMBLY A11, AND DISPLAY POWER SUPPLY ASSEMBLY A3, SCHEMATIC DIAGRAM (2 OF 2)

HIGH VOLTAGE POWER SUPPLY ASSEMBLY A4, CIRCUIT DESCRIPTION

WARNING

Hazardous voltages are present in this assembly.

High Voltage Power Supply Assembly A4 provides operating potentials for the cathode-ray tube (CRT). The nominal potentials are:

- Cathode, −2450 Vdc
- Control grid, −2500 Vdc
- Post accelerator (from High Voltage Quadrupler), +9000 Vdc
- Focus grid, −1650 Vdc
- Filament, 5.9 Vac floating at −2450 Vdc

Voltage potential for accelerator mesh, and adjustments for astigmatism and pattern are located on Display Power Supply Assembly A3.

+26V Filter Ⓐ

This circuit serves two purposes:

- Filtering by L1, L2, C1, and C2 reduces the level of the 40-kHz ripple (from the high-voltage oscillator) that is present in the power supply.
- Filtering by R1, C3, and the Darlington pair Q2 and Q3 removes the 120-Hz ripple on the +26V UNREG supply line before it is applied to the primary of the high-voltage transformer A1T1, thus reducing line-related intensity modulation.

Oscillator Driver Ⓑ

The collector of Q1 is connected to the primary winding of high-voltage transformer A1T1, and a feedback winding is connected to the base of Q1. Positive feedback from this winding causes the circuit to oscillate at a frequency (approximately 40 to 45 kHz) determined primariy by the characteristics of A1T1. Q1 operates as a Class C amplifier, supplying a current of about 2A peak over a conduction period of less than one-half cycle.

Oscillator Bias Current Regulator Ⓒ

Amplifier U1 regulates the dc level of the CRT cathode voltage by controlling the base drive to Q1 through the feedback winding. The cathode voltage is sampled via current through the Feedback circuit, which is compared with a reference current through R3 and R4 at U1 pin 3. The output of U1 drives the base of Q1 at the level (set by HV potentiometer R4) necessary to maintain about −2450 Vdc at the cathode of the CRT. Note that U1 does not switch at the 40-kHz rate. It controls the average bias current for the base of Q1, which controls its conduction period.

High Voltage Transformer Ⓓ

WARNING

The CRT filament potential is connected to the hazardous cathode potential of −2450 Vdc. Measurement of the filament voltage is not recommended, as most voltmeters are not rated to withstand a floating input of this magnitude.

Transformer A1T1 and transistor Q1 form an oscillator circuit whose power is provided by the +26V UNREG line. The primary winding is connected to the collector of Q1, and the feedback winding is connected to the base of Q1. A1T1 has two secondary windings: one supplies high voltage and the other, a filament voltage of 5.9 Vac to the CRT.

The high-voltage winding of A1T1 is tapped to provide a sine wave for the level shifters. The winding is also tapped at another point that is connected to the high-voltage multiplier, in which the voltage is quadrupled, rectified, and filtered. The resulting +9000 Vdc is applied to the post accelerator of the CRT. The full output of the secondary is rectified by A1CR1 and applied to the High Voltage Filter.

High Voltage Filter Ⓔ and Feedback Ⓕ

The components C9, C10, and R13 filter out the 40-kHz ripple on the rectified high voltage from the high voltage transformer. The output of the filter is a nominal −2450 Vdc whose value is set by HV potentiometer R4 to the value marked on A1T1. This sets the CRT filament voltage to 5.9 Vac, the potential required for maximum CRT life. The output of −2450 Vdc goes directly to the cathode of the CRT and floats the filament at the same potential via R12. The CONT GRID and FOCUS GRID voltages are derived from this voltage. Feedback current for the Oscillator Bias Current Regulator is provided through R14 and C12.

Control Grid Level Shifter Ⓖ

WARNING

Turn power off before connecting or disconnecting a test probe. TP5 in this block is located near high voltage.

The CONT GRID voltage is referenced to the CATH voltage with an intensity control bias developed by means of a level shift circuit. This bias voltage is generated by a sine-wave signal, from a tap on a secondary winding of A1T1, that is coupled through A1C1. The top and bottom of the sine wave are clipped, with the top being clipped by diode CR8. The upper clipping level is set by INT LIM potentiometer R18. The bottom of the sine wave is clipped by the action of diode CR11. The lower clipping level is set by the CONTROL GATE voltage from XYZ Amplifier Assembly A6. The clipped sine wave is coupled through C14 to the rectifier circuit CR9 and CR10 to generate a dc bias voltage across R21. The dc level established is negative with respect to the cathode and is applied to the CRT control grid. Capacitor C15 removes 40-kHz ripple from the bias voltage and allows fast pulse signals to be coupled directly to the control grid. Neon tubes VR3 and VR4 go into conduction if the cathode-to-grid potential is greater than about 180 Vdc. This provides protection to the CRT and associated circuitry, especially during instrument turn-off. Spark gaps are provided to protect components from possible arcing between electrodes in the CRT.

With the CONTROL GATE input at the maximum level of +70 Vdc, the maximum clipping of the bottom of the sine wave occurs. This results in the smallest peak-to-peak swing of the sine wave, since the upper clipping level is held constant by the intensity limit divider network. The rectified and clipped sine wave is then at its minimum dc value, providing the minimum reverse bias of the control grid with respect to the cathode voltage. This provides maximum CRT intensity.

CAUTION

Misadjustment of INT LIM potentiometer R18 can permanently damage the CRT, in as little as 10 seconds, by allowing the grid-to-cathode to be forward biased.

INT LIM potentiometer R18 is set so that a +30 Vdc level at the CONTROL GATE input corresponds to the CRT beam cutoff point. The maximum CONTROL GATE voltage is +70 Vdc at maximum intensity. At this maximum level of 40 Vdc above cutoff, the control grid is still reverse-biased by 20 Vdc to 50 Vdc, depending on the CRT.

The control grid must not be allowed to go positive with respect to the cathode. If this should happen, permanent damage to the CRT (a hollow cathode) can occur in as little as 10 seconds. The symptom of a hollow cathode is that increasing the front-panel INTENSITY control at some point causes the CRT intensity to diminish rather than to continue increasing.

Zener diode VR5 protects the CRT cathode from any excessive voltage on the CONTROL GATE line that might result from a failure or misadjustment in XYZ Amplifier Assembly A6. It has a voltage limit of 75 Vdc, which, even in the worst case, results in a grid-to-cathode reverse bias of 10 Vdc.

The CONTROL GATE level, and hence the CRT intensity, is a function of the front-panel INTENSITY control. In digital storage modes, this level is modulated by the trace stroke length and by the type of information being refreshed in the display; i.e., traces, characters, and graticule illumination.

Focus Grid Level Shifter H

WARNING

Turn power off before connecting or disconnecting a test probe. TP6 in this block is located near high voltage.

The FOCUS GRID voltage is set by a resistor divider string (R28, R29, R30, and front-panel FOCUS control) from the cathode with a dynamic focus correction bias developed by means of a level shift circuit. Zener diodes VR6 and VR7 clamp the FOCUS line voltage to +300 Vdc if the line should be opened. The wiper of FOCUS LIMIT potentiometer R29 is filtered by C18. The focus grid is a little more negative than this because of the bias voltage developed by the level shift circuit. This bias voltage is generated by a sine-wave signal from a tap on a secondary winding of A1T1. The signal is coupled through A1C2. The top and bottom of the sine wave are clipped, with the top being clipped by diode CR12. The upper clipping level is set at a fixed voltage by VR8. The bottom of the sine wave is clipped by the action of CR15. The lower clipping level is set by the FOCUS GATE voltage from XYZ Amplifier Assembly A6. The clipped sine wave is coupled through C19 to the rectifier circuit CR13 and CR14 to generate a dc voltage across R33. Capacitor C20 removes 40-kHz ripple from the bias voltage and also allows fast pulse signals to be coupled directly to the focus grid.

The FOCUS GRID signal provides dynamic focus correction to compensate for defocusing caused by changes in trace position and CONTROL GRID level. The CONTROL GRID level is itself dynamically changed as a function of trace stroke length. During the time the graticule illumination raster is being refreshed on the CRT, the FOCUS line is pulled to ground, defocusing the trace to give even background illumination.

Spark gaps are provided to protect components from possible arcing between electrodes of the CRT.

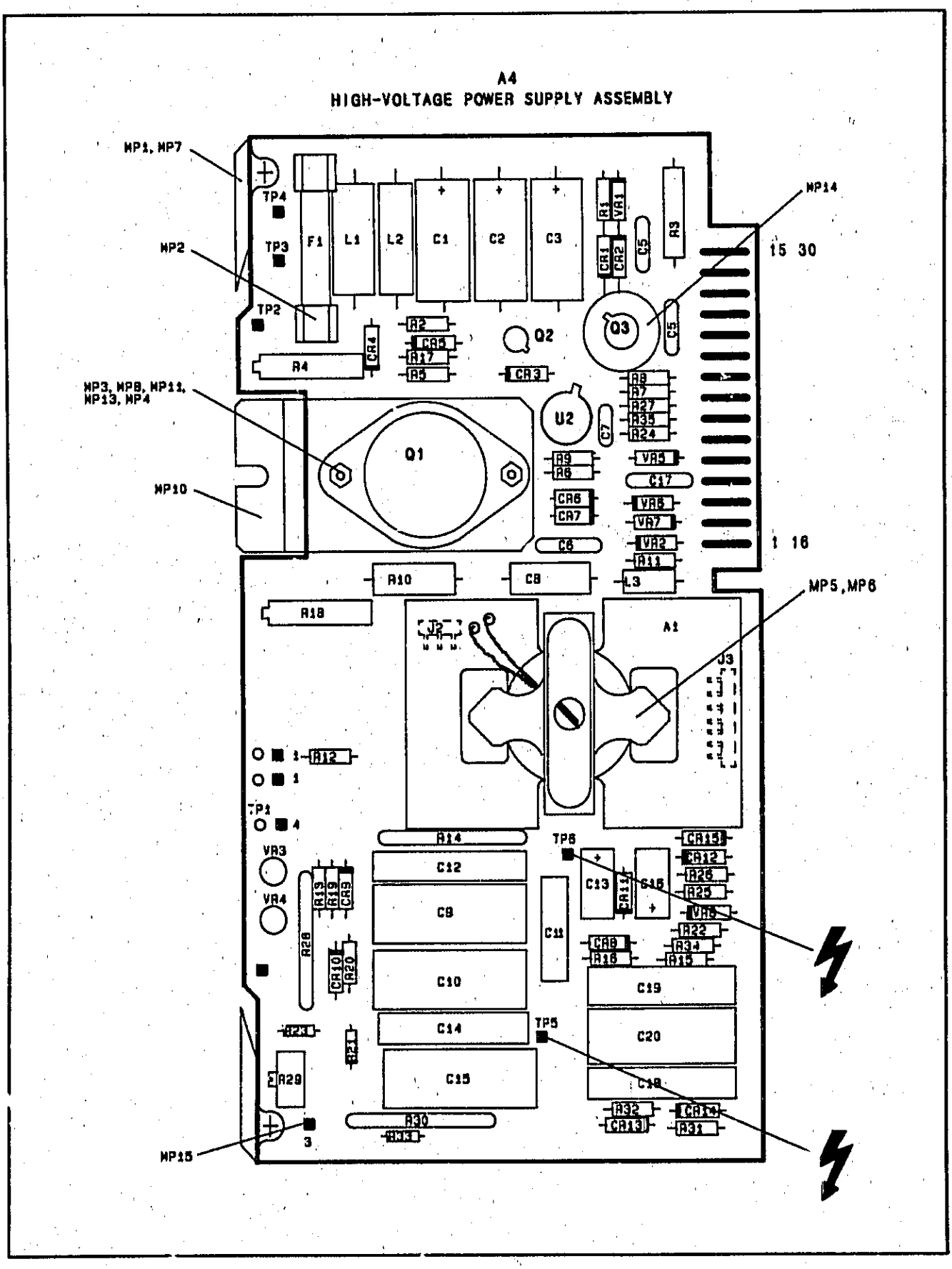


Figure 8-13. High-Voltage Power Supply A4, Component Locations

A4 HIGH-VOLTAGE POWER SUPPLY ASSEMBLY 08569-60005

WARNING

HAZARDOUS VOLTAGES ARE PRESENT ON THIS ASSEMBLY

P1

PIN	SIGNAL	TO/FROM	FUNCTION BLOCK
1	ANLG GND	NOTE 5	I
18	ANLG GND	NOTE 5	I
2	ANLG GND	NOTE 5	I
17	ANLG GND	NOTE 5	I
3	NC		
19	NC		
4	FOCUS	A3P3-8	H
22	FOCUS	A3P3-3	H
5	CONTROL GATE	A4J3-26	G
20	CONTROL GATE	A4P3-26	G
6	FOCUS GATE	A3P3-34	H
21	FOCUS GATE	A3P3-34	H
7	NC		
22	NC		
8	NC		
23	NC		
9	NC		
24	NC		
10	-15V	A3J2-7	I
25	-15V	A3J2-7	I
11	+15V	A3J2-6	I
26	+15V	A3J2-6	I
12	+150V SW	A5P1-20, 45	I
27	+150V SW	A5P1-20, 45	I
13	REG GND	NOTE 5	I
28	REG GND	NOTE 5	I
14	+26V UNREG	A3J2-4	A
29	+26V UNREG	A3J2-4	A
15	HV GND	NOTE 5	I
30	HV GND	NOTE 5	I

SERIAL PREFIX: 2223A

Ⓐ +26V FILTER

Ⓑ OSCILLATOR DRIVER

Ⓒ OSCILLATOR BIAS CURRENT REGULATOR

Ⓓ HIGH VOLTAGE TRANSFORMER

A4A1 HIGH-VOLTAGE TRANSFORMER ASSEMBLY 08569-60006

Ⓔ HIGH VOLTAGE FILTER

Ⓕ FEEDBACK

Ⓖ CONTROL GRID LEVEL SHIFTER

Ⓗ FOCUS GRID LEVEL SHIFTER

Ⓘ POWER SUPPLIES

P/O A2 DISPLAY ADJUST ASSEMBLY

P/O A3 DISPLAY POWER SUPPLY ASSEMBLY

P/O A2 DISPLAY ADJUST ASSEMBLY

WARNING

USE NON-METALIC TOOL ONLY

WARNING HIGH VOLTAGE

DISCONNECT AT CRT WITH CAUTION! DISCHARGE FIRST BY GROUNDING AT CRT CONNECTION!

NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. FOR COMPLETE REFERENCE DESIGNATOR, PREFIX ABBREVIATION WITH ASSEMBLY DESIGNATOR.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IS IN OHMS (Ω) CAPACITANCE IS IN MICROFARADS (μF) INDUCTANCE IS IN MICROHENRIES (μH)
3. UNLESS OTHERWISE INDICATED, SIGNALS ENTER AT LEFT SIDE AND EXIT AT RIGHT SIDE OF JUNCTION BLOCKS.
4. WARNING

   TURN POWER OFF BEFORE CONNECTING OR DISCONNECTING PROBE. TEST POINT IS NEAR HIGH VOLTAGE.
5. HC GND CONNECTS TO HIGH CURRENT GROUND (HC GND) AT PLUG-IN POWER SUPPLY A5, (SEE FIGURE 8-12.) REG GND AND ANLG GND CONNECT TO CHASSIS (GND) AT MOTHERBOARD.
6. MNEMONIC TABLE:

MNEMONIC	DESCRIPTION
ACCEL	ACCELERATOR MESH
ASTIG	ASTIGMATISM
REG GND	REGULATOR GROUND
HC GND	HIGH CURRENT GROUND
HV	HIGH VOLTAGE
INT LIM	INTENSITY LIMIT
+150V SW	+150V SWITCHED

7. TEST POINTS 1 THROUGH 5 ARE SHOWN WITH UNBLANK IN ANALOG DISPLAY MODE. FOR OTHER MEASUREMENT CONDITIONS, SEE FIGURE 8-3.

CRT CONNECTOR (REAR VIEW)

A4

FIGURE 8-14. HIGH-VOLTAGE POWER SUPPLY ASSEMBLY A4, SCHEMATIC DIAGRAM

DATA CONVERTER ASSEMBLY A5, CIRCUIT DESCRIPTION

The Data Converter circuit has four major functions. First, it converts vertical analog information (VIDEO) from the RF plug-in to digital information (stroke data) for storage in Stroke Memory (A7). The Maximum Peak Detector, Minimum Peak Detector, Multiplexer, Analog to Digital Converter, and Decoding and Timing circuits perform this function, according to instructions from the Decoding and Timing circuit, which is controlled by the Processor Assembly, A7.

Second, the Data Converter processes stroke data from Stroke Memory to form the vertical deflection signal (DGTL Y) for the CRT. The Y Data Buffer and Digital Y Generator accomplish this function.

Third, the Digital X Generator generates a ramp (DGTL X) which sweeps the CRT beam horizontally for trace A, trace B, characters, and graticule illumination.

Fourth, Z Modulation modulates the CRT beam intensity so that short and long strokes have the same brightness (STROKE LEN).

Maximum Peak Detector (A)

The Maximum Peak Detector monitors the VIDEO input signal and holds its maximum input level until it is reset. Decoding and Timing resets the peak detector according to commands from Processor Assembly A7. A simplified schematic of the Maximum Peak Detector circuit is shown in Figure 8-15.

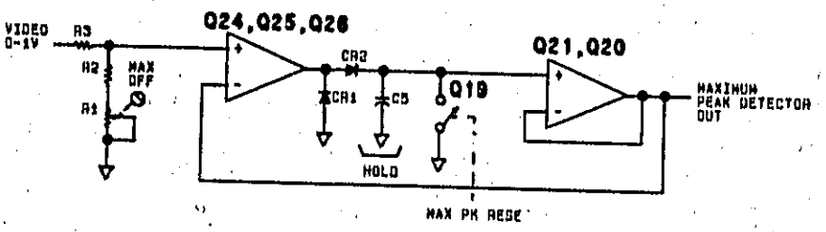


Figure 8-15. Simplified Maximum Peak Detector Schematic

The VIDEO input signal is fed to emitter follower Q24. (See detailed schematic, Figure 8-26.) When the VIDEO input is a positive-going voltage (more positive than the previous maximum), CR2 is forward biased, and hold-capacitor C5 is charged to a higher value. Since the gate of Q21B is tied to its source, the voltage at the source of Q21A is the same as the voltage at its gate. This voltage appears (after two emitter-base voltage drops) at the right side of differential pair Q26A and Q26B. MAX OFF potentiometer R1 adjusts the offset of this circuit for a gain of 1. U12 buffers the output.

MAX PK RESET from Decoding and Timing resets the Maximum Peak Detector. A 200ns, negative-going pulse from the MAX PK RESET line turns off Q18, allowing the gate of Q19 to be forward biased by +11V, through R14 and R15. The pulse turns on Q19 for a period of 200 ns and discharges C5.

U32 compares the input and output of the peak detector. A TTL high level is produced when the input is less than the output.

Minimum Peak Detector (B)

The Minimum Peak Detector monitors the VIDEO input signal and holds its minimum input level until it is reset. Circuit operation is the same as that of the Maximum Peak Detector except that supply polarities are reversed and PNP transistors are used instead of NPN transistors. A simplified schematic of the Minimum Peak Detector is shown in Figure 8-16.

When the VIDEO input is a negative-going voltage (more negative than the previous minimum), CR4 is forward biased and hold-capacitor C14 is charged to a more negative value. CR14 (see Figure 8-26) creates an

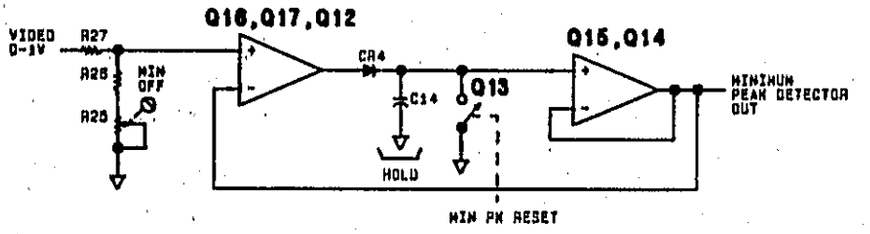


Figure 8-16. Simplified Minimum Peak Detector Schematic

offset between the output and the emitter of Q14. This ensures that the voltage across C14 is always negative for positive outputs from 0V to +1V. MIN OFF potentiometer R25 adjusts the offset of the Minimum Peak Detector. U13B compares the input to the output.

MIN PK RESET resets the Minimum Peak Detector. A negative-going pulse from the MIN PK RESET line turns on Q13, causing C14 to discharge.

Decoding and Timing D

This circuit provides timing for the Maximum Peak Detector, the Minimum Peak Detector, and the Track and Hold circuits.

Initially, the processor requests a conversion, setting the REQ CONV line high. The D flip-flop, U30, delays the REQ CONV signal until it is clocked by a positive-going CNT1 signal. This delayed REQ CONV signal becomes the HOLD signal. When HOLD is high, it instructs the Track and Hold circuit to hold its peak value.

The HOLD signal also triggers a one-shot multivibrator, U29A, which produces a 200 ns pulse. This pulse is timing for the reset pulses that control the discharge of the hold-capacitors in the maximum and minimum peak detectors N P . The timing pulse passes to NAND gates U19A and U19C, together with Processor Assembly control lines IN SEL A and IN SEL B, which steer the reset pulses to either the Minimum Peak Detector or the Maximum Peak Detector. See Table 8-4 and Figure 8-17.

Table 8-4. Peak Detector Reset Pulses

	IN SEL A	IN SEL B
Minimum Detector Enabled	0	1
Maximum Detector Enabled	1	0
VIDEO (Analog mode) Both detectors disabled	0	1
SWEEP (Analog mode) Both detectors disabled	1	1

U29B is a one-shot multivibrator, which is triggered by the 200 ns timing pulse. The U29B output of 500 ns goes to NAND gates U20A and U20B, together with inputs from comparators U13 and U32. When the 500 ns pulse is high, a high from comparators U13 and U32 will set flip flops U31A and U31B, respectively. This indicates that the VIDEO signal level rose and fell, indicating it has noise characteristics: L NOISE is low.

When L NOISE is low, the CPU (A7) determines the amplitude of the noise display by sampling the minimum and maximum peak detector outputs.

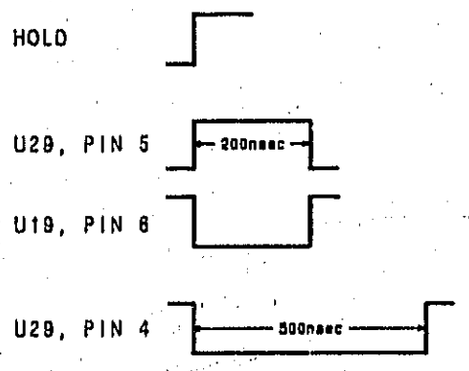


Figure 8-17. Data Converter Timing

Multiplexer ⓔ

The Multiplexer switches inputs to the Track and Hold circuit, according to the logic states of IN SEL A and IN SEL B. The signals switched are the outputs of the maximum or minimum peak detectors, VIDEO, or SWEEP. Table 8-5 is a truth table for the Multiplexer.

Table 8-5. Multiplexer Truth Table

IN SEL A	IN SEL B	MULTIPLEXER OUTPUT (PIN 13)
0	0	Minimum Peak Detector
1	0	Maximum Peak Detector
0	1	VIDEO
1	1	SWEEP

The components at pins 7 and 16 of U10 are voltage dividers and filters for the U10 power supplies.

The SWEEP input is attenuated and offset by divider networks R52 and R53, and R50 and VR1. The sweep ramp, −5V to +5V, is changed to a ramp of 0V to +1V. VR1 is temperature compensated.

Track and Hold ⓕ

This circuit holds or tracks its input signal (maximum or minimum peak detector outputs, VIDEO, or SWEEP.) Figure 8-18 is a simplified schematic of the circuit.

When tracking, HOLD (from Decoding and Timing) is low, Q7 is off, and FET switch Q8 is on (closed). (See Figure 8-26.) The voltage across C28 tracks the input voltage. The capacitor voltage passes to the high impedance X10 amplifier formed by Q10A, Q10B, U9, and resistors R69, R70, and R71.

When the Track and Hold circuit is holding, HOLD is high. Q7 is on, and FET switch Q8 is off (open). The input signal charges hold-capacitor C28, and C28 holds its charge.

U9 maintains equal voltages at the gates of Q10A and A10B. As U9 amplifies its input by 10, it varies the voltage at the gate of Q10B to maintain equal current through identical resistors, R67 and R68. When the input exceeds about 1.2 volts, U9 begins to saturate, and it can no longer maintain equal current through R67 and R68; the voltage at its inputs begins to differ. CR15 limits the difference between the U9 inputs to 0.6 volts.

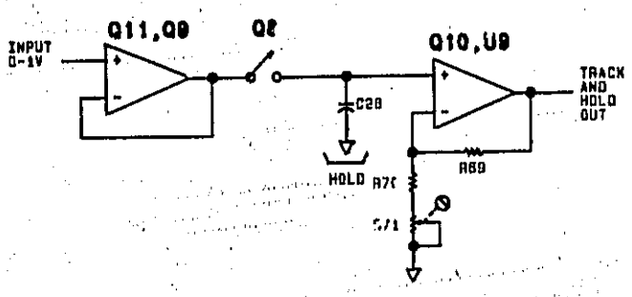


Figure 8-18. Simplified Track and Hold Schematic

U9 is normally not saturated because the input signals from the Multiplexer usually do not exceed 1.2V. The −5V to +5V sweep signal is attenuated to a 0V to +1V ramp in the Multiplexer circuit. Vertical signals from the minimum and maximum peak detectors, and the VIDEO signal can exceed 1.2 volts when the spectrum analyzer display scale is set to 1 dB/DIV.

Q11A, Q11B, and Q9 form an input voltage follower.

Analog to Digital Converter ⓕ

The Analog to Digital Converter converts the analog voltage from Track and Hold to digital information. The CPU stores this data in Stroke Memory (A7).

Using internal sensing resistors, U6 senses the analog voltage from Track and Hold and a programmed current from the successive approximation register, U8. The resulting currents are compared in U6 and the difference generates an error voltage at pin 15. The error voltage causes comparator U7 output to go high or low. The comparator output, fed back to U8, determines whether the bits that generated the programmed current in U6 should be a high or low state.

When HOLD is high, the successive approximation register (SAR) cycle begins. Initially, all of the output bits from U8 are set high. Then each of the bits is set low one at a time, successively from the most significant bit (MSB) to the least significant bit (LSB). The value of the SAR output changes by one half, as each bit is set low. As each bit is set low, U6 compares the analog voltage from the Track and Hold circuit to the programmed current from the SAR. If the current produced by the analog voltage is lower than the programmed current, comparator U7 output is low. The U7 output is fed back to the SAR. If the output of U7 is low, the data bit in the SAR that was set low, remains low. If the output of U7 is high, the data bit in the SAR that was set low, becomes high. The next bit is then set low, and the comparison process begins again. The ADC BUSY line signals the completion of the conversion.

CNT 1 is the clock for this process. When the HOLD signal is low, U8 is reset.

Since the CPU in Processor Assembly A7 can process only 8 bits of data at a time, the 10 bits of data are changed to one 8-bit byte and one two-bit nibble. When ADC HI BYTE is high (address $1), 3-STATE buffers U27 and U28 output the eight high order bits to the Data Bus. When ADC LO BYTE is high (address $0), U27 outputs the two low order bits to the Data Bus.

Y Data Buffer ⓗ

The Y Data Buffer routes data from the Data Bus to the Digital Y Generator ⓖ and Z Modulation ⓘ. It processes 11 bits of data: 10 bits of vertical display information and 1 bit of blanking information. It stores this data temporarily on scratch pad memories U21, U22, and U23, which are 16 bit (4 x 4) RAMs. STRK DATA STRB write-enables the RAMs. STROKE SEL selects the output which is read by digital to analog converters U14 and U1. STROKE SEL, after inversion by U17, chooses the set of inputs onto which the Data Bus writes.

Inputs to DAC U14 are the most significant eight bits of data from buffers U21 and U22. U14 converts this digital data to analog current. This current passes to the Z Modulation circuit ⓘ.

Digital Y Generator H

Data from the Y Data Buffer provides vertical display information which represents the traces on the CRT. The Digital Y Generator circuit generates a vertical signal for the CRT when the instrument is in the digital display mode.

The HP 853A Display mainframe draws 512 strokes per sweep: one stroke for every bucket of the horizontal axis. The Digital Y Generator determines the slope of each stroke by comparing the vertical value of the last bucket, to the vertical value of the next bucket. The difference in value is proportional to the slope of the trace.

A simplified schematic is shown in Figure 8-19. DAC U1 provides an output current proportional to the vertical value of the next bucket. A current proportional to the vertical value of the last bucket is produced in R99 and R100 when C47, the hold capacitor, is charged through Q1 during the sample interval. The currents are summed in a current node at the source of Q4. The summed current is passed to integrator U3 which produces a ramp. The ramp, DGTL Y, has a slope proportional to the difference between the currents at the summing node.

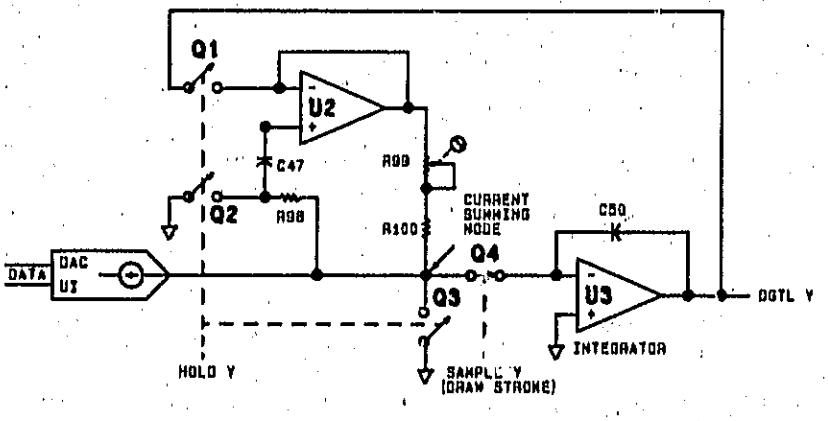


Figure 8-19. Simplified Digital Y Generator Schematic

DGTL Y is produced in two steps. In the first step, the circuit is holding the last value of Y. STRK GEN TIMG from the Processor Assembly is low for 1 μs, and FET switches Q1, Q2 and Q3 are on (closed). (See Figure 8-20.) The output of U3, the last value of Y, is stored on C47. FET switch Q4 is off (open).

In the second step the circuit is sampling current. STRK GEN TIMG is high for 6 μs, and Q1, Q2 and Q3 are off. Q4 is on. (See Figure 8-21.) The voltage stored on C47 during the hold interval now appears across R99 and R100. The current through R99 and R100 is added with current from U1 at the source of Q4, and is passed to the integrator, U3. U3 produces a ramp, DGTL Y.

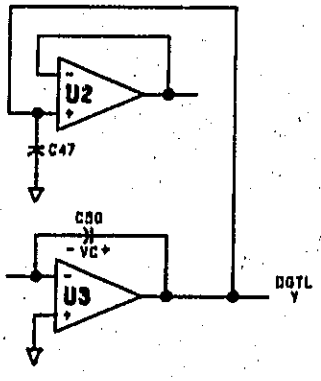


Figure 8-20. Holding Y

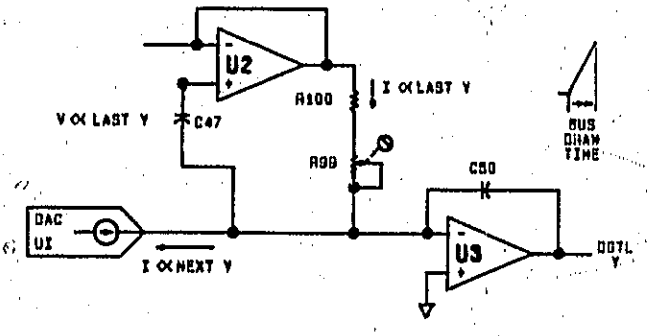


Figure 8-21. Sampling Y

An RLC network is formed by R117, L7, and C47, which allows C47 to charge and stabilize in 1 μs.

Potentiometer R97, Y GAIN, adjusts the DAC current that represents full vertical scale deflection.

Transistor Q3 minimizes leakage through Q4, during the period when C47 is holding.

Z Modulation

The Z Modulation circuit varies the intensity of the CRT trace according to the stroke length, so that both long and short strokes have the same brightness.

The Z Modulation circuit acts as an absolute magnitude detector. The outputs of DAC U14 and U2 are proportional to the positions of the next data point and last data point, respectively. These outputs are summed at the input of U15. The current at the summing node is bidirectional and is converted to a unidirectional voltage, which is proportional to the length of the trace.

Figure 8-22(A) represents the Z Modulation circuit when the net current at the summing node is moving away from the input of U15. The output of U15 becomes positive, turning CR13 on. The voltage out of U16 is equal to the voltage at its input plus the voltage across R109, or I x R109.

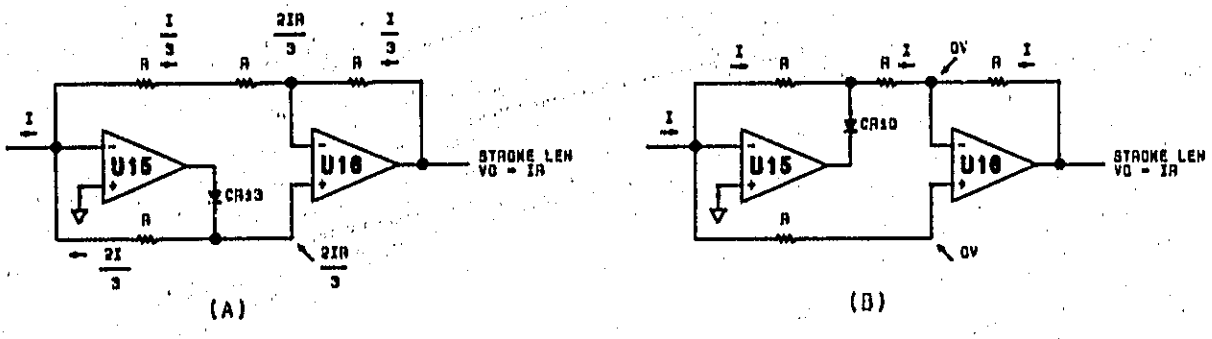


Figure 8-22. Simplified Z Modulation Schematic

Figure 8-22(B) represents the Z Modulation circuit when the net current at the summing node is moving toward the input of U15. The output of U3 becomes negative, turning CR10 on. The voltage out of U16 is equal to the voltage across R109, or I x R109.

C83 provides high frequency compensation.

R104, INTEN EQ, adjusts intensity evenness for long and short strokes.

Digital X Generator

The Digital X Generator produces the sawtooth ramp, DGTL X. The display sequence is trace A, graticule illumination, trace B, and characters. (See Figure 8-23.) This sequence repeats itself continually at an approximate rate of 55 Hz, and should not be confused with the sweep rate controlled by the front-panel SWEEP TIME/DIV control. Traces A and B are swept from right to left. Graticule illumination and characters are swept from left to right.

U26 and C41 form the integrator that produces the DGTL X sawtooth ramp. The slope of the ramp is varied by the currents through resistors R85, R86, and R87, which are summed at the source of Q23. (See Figures 8-24 and 8-26.)

U4A and U4B are voltage sources for the bias currents through R85, R86, and R87. The voltage from U4A is routed by multiplexer U5 to either R86 or R87, depending on the states of DSPL TRACE and DSPL CHAR.

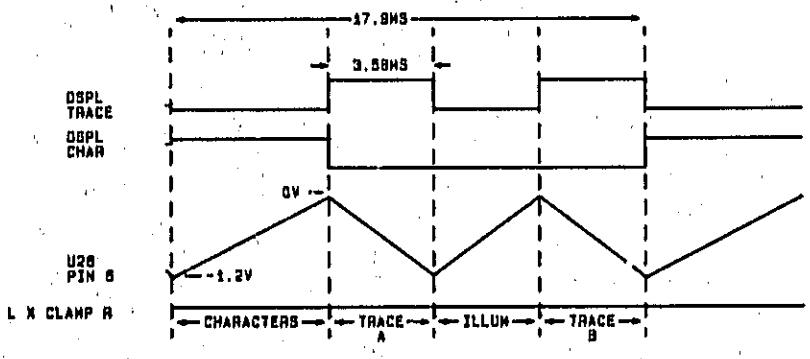


Figure 8-23. Digital X Generator Timing

U5 is a CMOS device. It reacts to input logic levels by pulling its corresponding outputs to its supply voltage levels, which are approximately +5V and ground. If the input voltage exceeds +2.5V, the output voltage is +5V; if the input voltage is less than +2.5V, the output is at ground. U4B is the voltage source for the bias current through R85.

The L X CLAMP R line resets the integrator output to 0V, so that traces A and B always start at the same place at the right side of the CRT display. When L X CLAMP R is low, Q5 turns on and CR11 is reverse-biased. This turns on Q22, discharges C41, and sets U26 output to 0V.

The X HOLD LEFT line opens the input to integrator U26, thus stopping the ramp output. This ensures that the first character displayed is always positioned at the left side of the CRT display. When X HOLD LEFT is high, Q6 is off and Q23 is on; the summed currents from R85, R86, and R87 pass to U26 and are integrated. When X HOLD LEFT is low, Q6 is on, turning off Q23; the current path to the U26 input is opened, and integration stops.

The X HOLD LEFT signal is active during mixed mode only, at sweep speeds of 5 ms/DIV or faster (10 ms/DIV or faster if in digital average display mode). At these sweep times, there is insufficient time for digital display circuitry to convert analog information to digital data and store it. To maintain display information, a mixed mode takes place in which both analog and digital information are displayed on the CRT: the graticule illumination and characters are digital information; traces A and B are analog information (VIDEO) from the spectrum analyzer plug-in. A number of complete sweeps must be displayed to maintain uniform brightness of the analog trace. Q23 is held open by the X HOLD LEFT. This delays the start of character sweep until X HOLD LEFT returns to its normally low state. (For detailed description, refer to Counter section of Processor Assembly A7 circuit description.)

The ramp out of integrator U26 is from −1.0V to 0V. The X OFF adjustment in resistor divider network R91, R92 and R93 shifts the ramp by 1V, changing the output to 0V to +1.0V at TP4 (DGTL X).

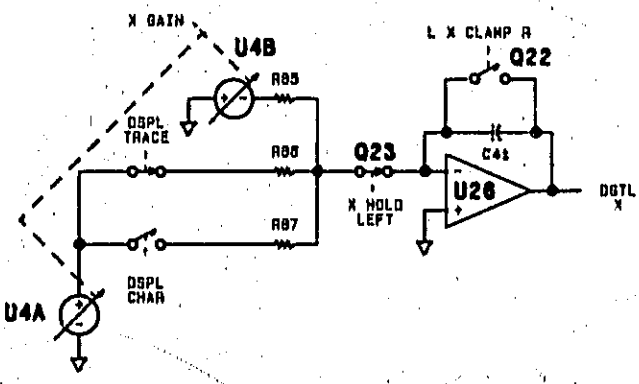


Figure 8-24. Simplified Digital X Generator Schematic

A5
DATA CONVERTER ASSEMBLY
00853-60007

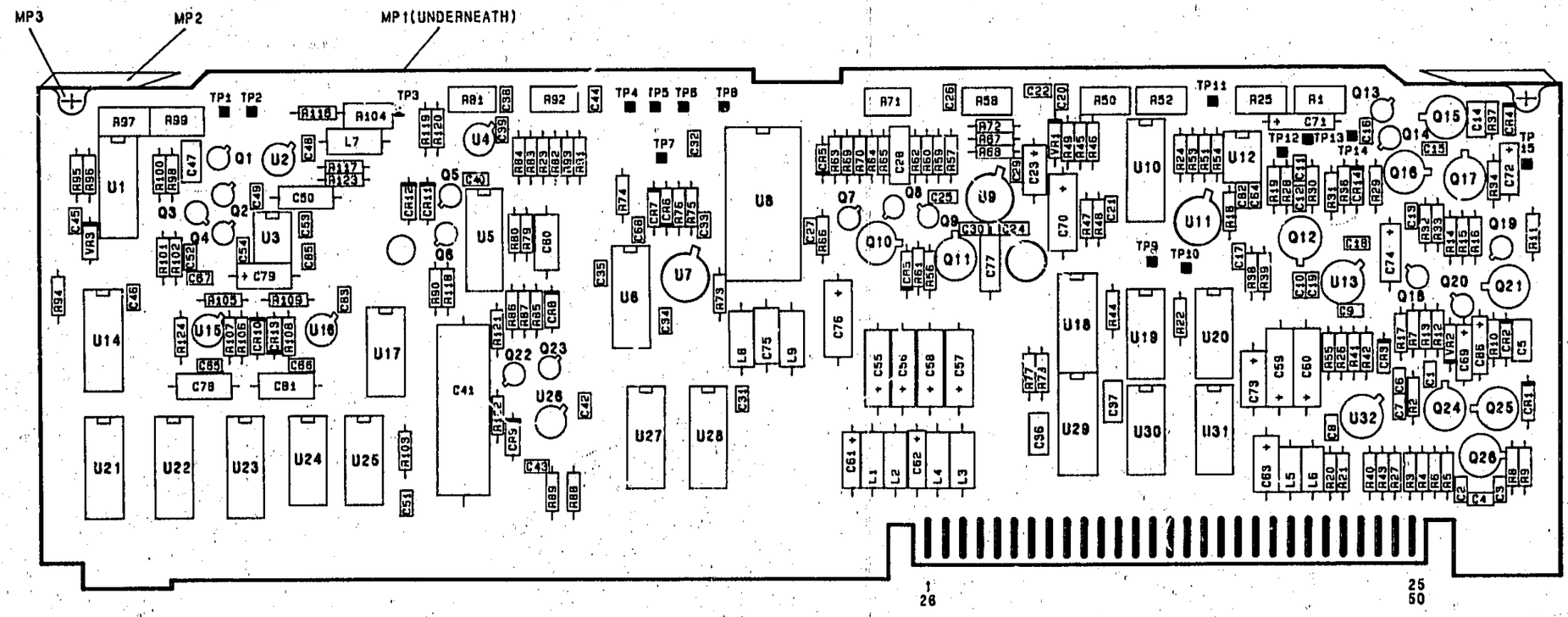
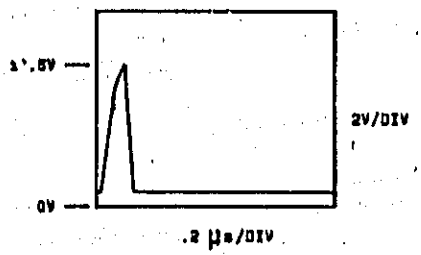
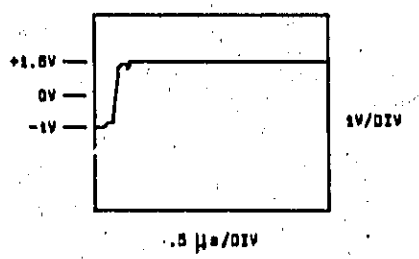


FIGURE 8-25. DATA CONVERTER ASSEMBLY A5, COMPONENT LOCATIONS

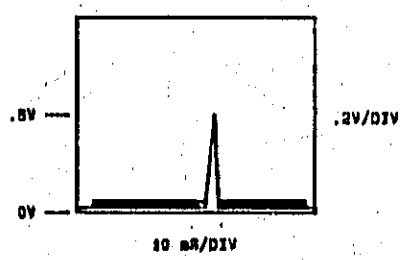
TEST POINT 15



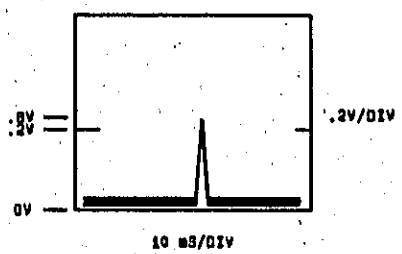
TEST POINT 14



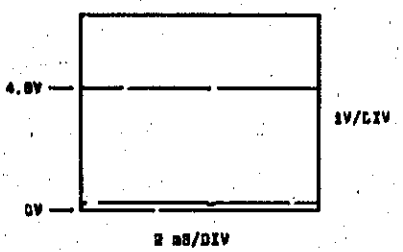
TEST POINT 12



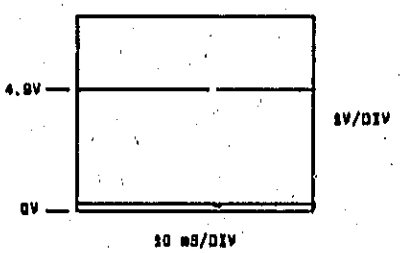
TEST POINT 11



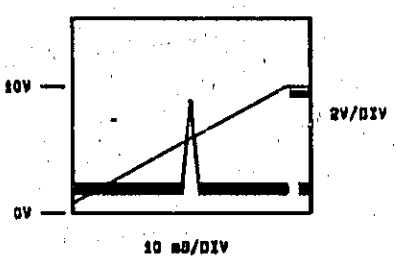
TEST POINT 10



TEST POINT 9



TEST POINT 6



SEE NOTE 6

SERVICE INFORMATION

CON'T

A5 DATA CONVERTER ASSEMBLY 00853-60007 (SHEET 1 OF 2)

P1

PIN	SIGNAL	TO/FROM	FUNCTION BLOCK
1 26	+15V +15V	A3J2-8 A3J2-9	K K
2 27	ANLG GND ANLG GND	NOTE 5 NOTE 5	K K
3 28	-15V -15V	A3J2-7 A3J2-7	K K
4 29	DGTL Y DGTL X	A3P1-18 A3P1-43	H J
5 30	STROKE LEN DSPL CHAR	A3P1-35 A7J2-12	I J
6 31	L X CLAMP R DSPL TRACE	A7J2-14 A7J2-13	J J
7 32	STRK BLNK LEND STROKE BLNK	A7J2-16 A7J23-15	G G
8 33	STRK GEN TIMG STRK DATA STRB	A7J2-19 A7J2-17	H G
9 34	X HOLD LEFT STROKE DEL	A7J2-21 A7J2-10	J G
10 35	D7 D8	A3J2-23 A3J2-22	G G
11 36	D6 D5	A3J2-25 A3J2-24	F, G F, G
12 37	D11 D10	A3J2-27 A3J2-26	F, G F, G
13 38	D13 D12	A3J2-29 A3J2-28	F, G F, G
14 39	D15 D14	A3J2-31 A3J2-30	F, G F, G
15 40	ADC HIBYTE ADC BUSY	A7J2-35 A7J2-33	F F
16 41	IN SEL A ADC LOBYTE	A7J2-39 A7J2-37	F, D F
17 42	REQ CONV IN SEL B	A7J2-41 A7J2-40	D C, D
18 43	ADC CLK NC	A7J2-44	F, D
19 44	LNOISE SWEEP	A7J2-43 A8P2-42, A8J2-14	D C
20 45	BUFFER GND BUFFER GND	NOTE 5 NOTE 5	K K
21 46	+5V +5V	A3J2-12, 13,14	K K
22 47	DGTL GND DGTL GND	NOTE 5 NOTE 5	K K
23 48	NC NC		
24 49	NC NC		
25 50	RETURN VIDEO	NOTE 5 A8P1-50 A8J2-15	K A, C

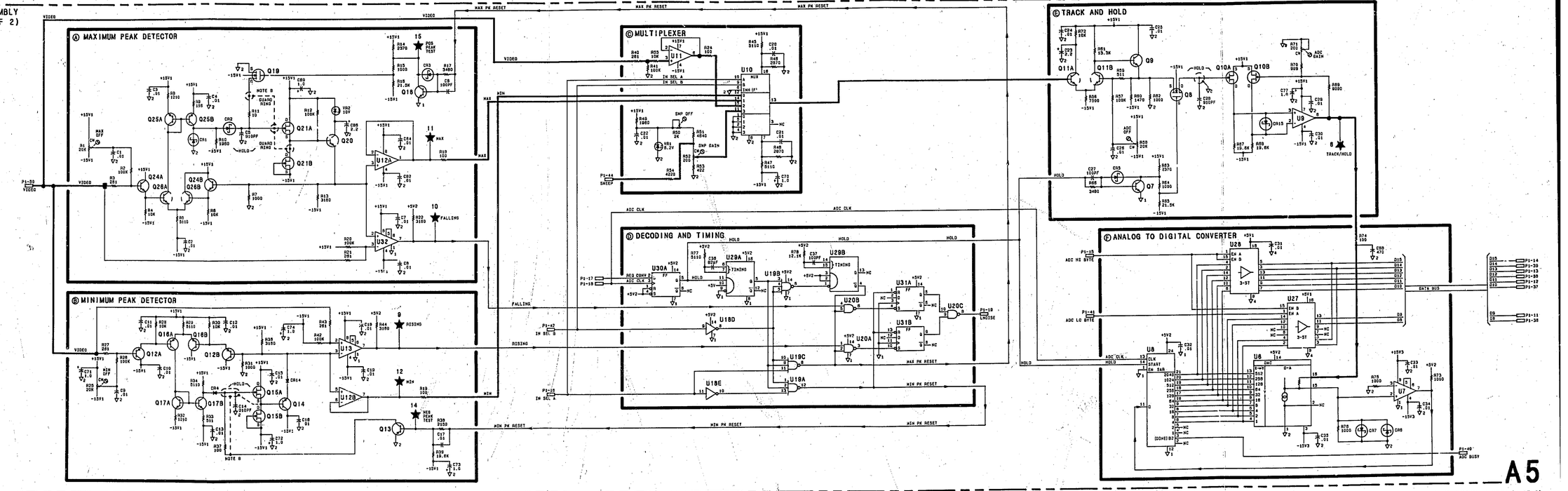
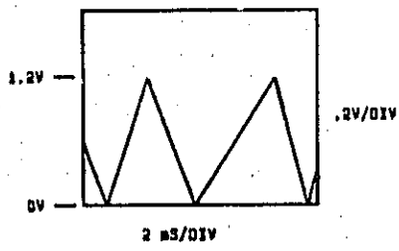


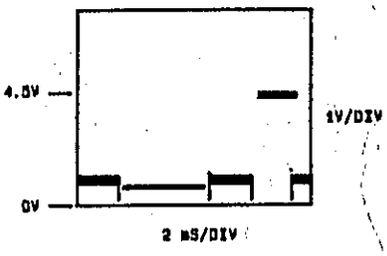
FIGURE 8-26. DATA CONVERTER ASSEMBLY A5, SCHEMATIC DIAGRAM (1 OF 2)

SERIAL PREFIX: 2223A

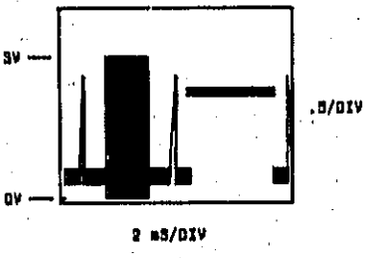
TEST POINT 4



TEST POINT 3

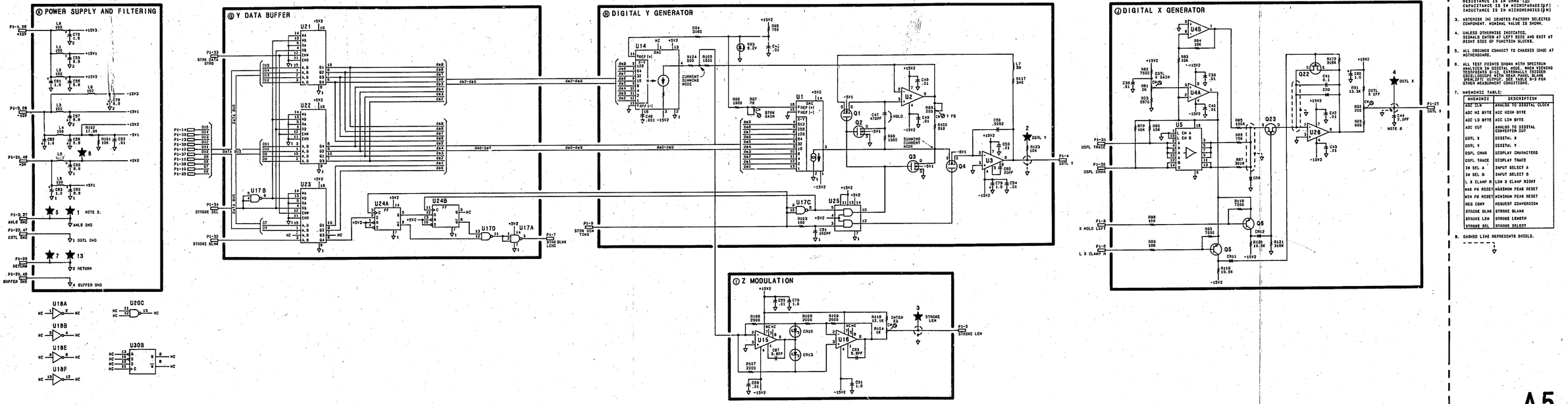


TEST POINT 2



SEE NOTE 6

A5 DATA CONVERTER ASSEMBLY
00853-60007 (SHEET 2 OF 2)



NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. FOR COMPLETE REFERENCE DESIGNATION, PREFIX ABBREVIATION WITH ASSEMBLY DESIGNATION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IS IN OHMS (Ω) CAPACITANCE IS IN MICROFARADS (μF) INDUCTANCE IS IN MICROHENRIES (μH)
3. ASTERISK (*) DENOTES FACTORY SELECTED COMPONENT. NOMINAL VALUE IS SHOWN.
4. UNLESS OTHERWISE INDICATED, SIGNALS ENTER AT LEFT SIDE AND EXIT AT RIGHT SIDE OF FUNCTION BLOCKS.
5. ALL GROUNDS CONNECT TO CHASSIS (GND) AT MOTHERBOARD.
6. ALL TEST POINTS SHOWN WITH SPECTRUM ANALYZER IN DIGITAL MODE, WHEN VIEWING TRIGGERED BY DSPL TRACE, WITH DISPLAY INTENSITY SET FOR NORMAL BRIGHTNESS (SPECIFIC OUTPUT: SEE TABLE 8-3 FOR OTHER MEASUREMENT CONDITIONS).
7. MNEMONIC TABLE:

MNEMONIC	DESCRIPTION
ADC CLK	ANALOG TO DIGITAL CLOCK
ADC HI BYTE	ADC HIGH BYTE
ADC LO BYTE	ADC LOW BYTE
ADC OUT	ANALOG TO DIGITAL CONVERSION OUT
DSTL X	DIGITAL X
DSTL Y	DIGITAL Y
DSPL CHAR	DISPLAY CHARACTERS
DSPL TRACE	DISPLAY TRACE
IN SEL A	INPUT SELECT A
IN SEL B	INPUT SELECT B
L X CLAMP B	LOW X CLAMP RIGHT
MAX PK RESET	MAXIMUM PEAK RESET
MIN PK RESET	MINIMUM PEAK RESET
RES CONV	REQUEST CONVERSION
STROKE BLNK	STROKE BLANK
STROKE LEN	STROKE LENGTH
STROKE SEL	STROKE SELECT

8. DASHED LINE REPRESENTS SHIELD.

A5

FIGURE 8-28. DATA CONVERTER ASSEMBLY A5, SCHEMATIC DIAGRAM (2 OF 2)

XYZ AMPLIFIER ASSEMBLY A6, CIRCUIT DESCRIPTION

The XYZ Amplifier Assembly amplifies analog or digital signals to drive the horizontal and vertical deflection plates of the CRT. DGTL Y, VIDEO, DGTL X and SWEEP are amplified in voltage to current converters and then in current to voltage converters before passing to the CRT deflection plates.

So that characters, scale illumination, and traces will have proper intensity and focus, this assembly modulates Z-Axis intensity and focus according to modulation and blanking signals from the Processor, Data Converter, and Interface Assemblies. The Voltage to Current Converter, Z-Axis converts modulation voltages to current sources. These current sources are summed and amplified in current to voltage converters that drive the control and focus grids of the CRT.

Digital/Analog Switch (X and Y) Ⓐ

This switch steers VIDEO or DGTL Y to the Voltage to Current Input Amplifier, Y-Axis Ⓑ, and SWEEP or DGTL X to the Voltage to Current Input Amplifier, X-Axis Ⓒ. See Figures 8-27 and 8-34.

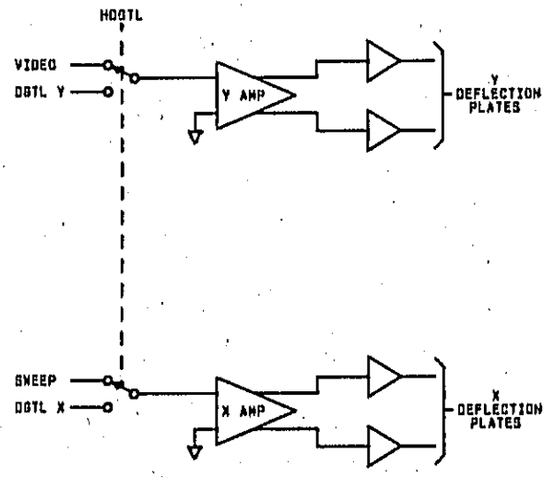


Figure 8-27. X and Y Amplifiers

Switch U2 contains four single-pole, single-throw, JFET analog switches connected as two double-pole, double-throw switches. U2B and U2C are normally closed. U2A and U2D are normally open.

When digital display modes are selected, or during character and graticule illumination display when in mixed mode, HDGTL is high. DGTL Y and DGTL X from Data Converter Assembly A5 pass to the Voltage to Current Input Amplifiers. (For detailed description of mixed mode, refer to Counter section in Processor Assembly A7 circuit description.)

When analog display mode is selected, HDGTL is low and VIDEO and SWEEP pass to the Voltage to Current Input Amplifiers.

Voltage to Current Input Amplifier, Y-Axis Ⓑ

This circuit converts its input voltage to two current sinks which drive the Output Driver Amplifier A, Y Axis and Output Driver Ampifier B, Y Axis. The nominal input is 0V to +.8V. The two current sinks are proportional to the voltages present at the two CRT deflection plates. These current sinks are complimentary and are produced by a series of differential amplifiers. See Figure 8-28.

Figure 8-28 shows the Voltage to Current Input Amplifier containing three differential pairs. To understand the amplifier, first assume that the base of Q5 is at 0V and bias resistors R19* and R21* are equal. For this case, the entire amplifier is balanced and output currents I_1 and I_2 are equal.

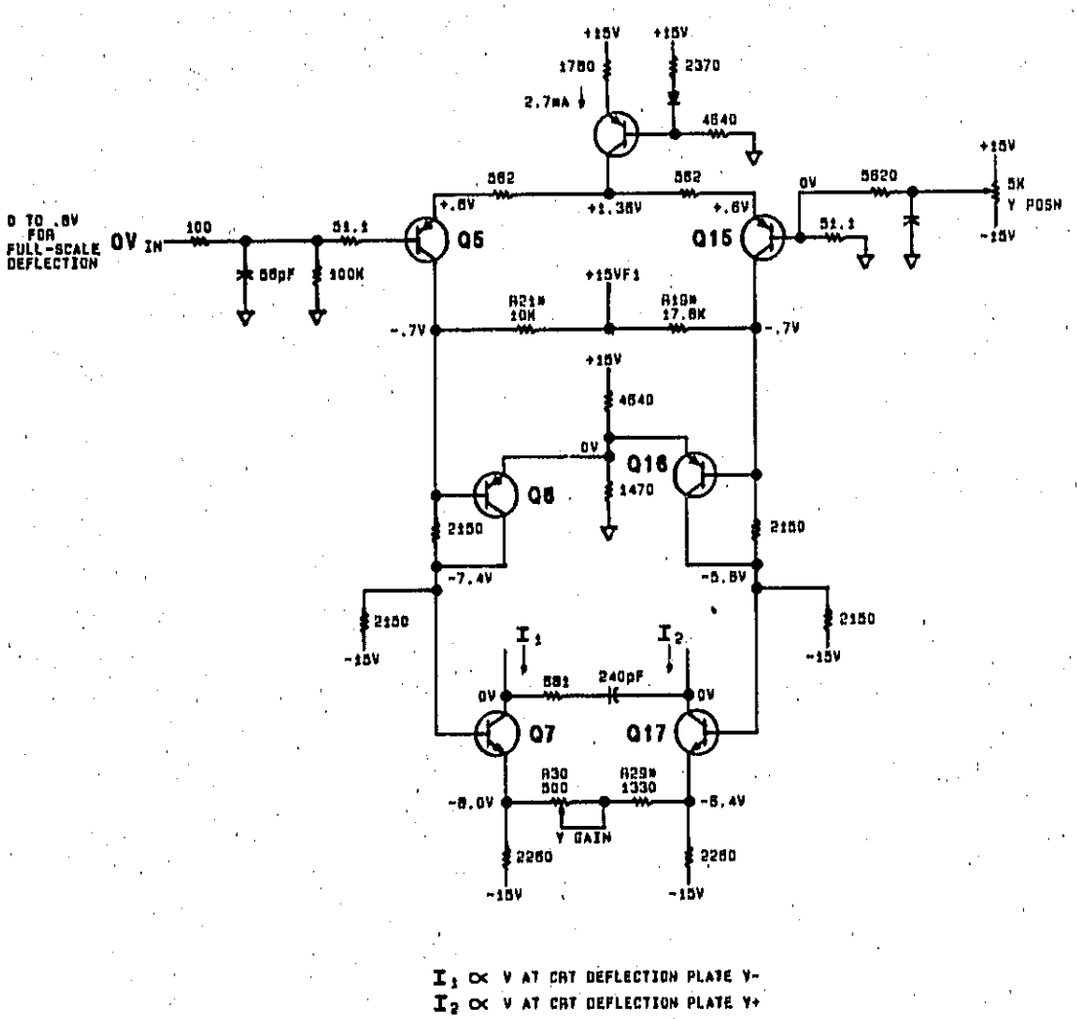


Figure 8-28. Voltage to Current Input Amplifier, Y Axis

In the actual circuit, R19* and R21* are not equal. Full screen deflection occurs when VIDEO (or DGTL Y) is at 0.8V. Midscreen deflection occurs when 0.4V is present at the base of Q5.

Ideally, R19* and R21* are selected so that the collector voltages of Q6 and Q16 are equal and the output currents, I_1 and I_2, are equal when 0.4V is present at the base of Q5. In practice, however, the resistors are selected to provide midscreen CRT deflection with 0.4V applied.

Voltage levels for troubleshooting are indicated on the XYZ Amplifier Schematic, Figure 8-34, and on Figure 8-28. For these measurements, first put the HP 853A in digital display mode and then short the base of Q5 to ground. This unbalances the output current I_1 and I_2, and causes the CRT beam to be at the bottom of the CRT display, if the amplifier is operating correctly. Since the amplifier stages are dc coupled, any errors present in one stage will be repeated in following stages.

All six stages have current gain, but only Q6 and Q16 have significant voltage gain.

Front panel control, Y POSN, varies the base voltage of Q15 by a few tenths of a volt. This offsets the amplifier to adjust CRT beam reflection.

Y GAIN adjustment R30 compensates for varying deflection factors of different CRTs. Resistor R29* is selected to optimize the range of R30.

Voltage to Current Input Amplifier, X Axis ⓒ

This circuit operation is identical to the Voltage to Current Input Amplifier, Y Axis, except that the nominal input voltage range is from 0V to +1.0V. Grounding the base of Q26 causes the CRT beam to go to the left of the display if the amplifier is operating correctly.

Output Driver Amplifier A, Y-Axis ⓓ
Output Driver Amplifier B, Y-Axis ⓔ

These two amplifiers are current to voltage amplifiers and are identical. Amplifier A is driven by Q17, which is the non-inverting output of the Voltage to Current Input Amplifier, Y-Axis. Amplifier B is driven by the inverted output, Q7. Amplifiers A and B are both wideband, inverting amplifiers that drive the CRT vertical deflection plates. Amplifier A is described.

Emitter follower Q19 can be ignored as a current path for low frequency operation. It is ac coupled to Q8 and Q21 to improve the high frequency performance of the circuit.

First, assume that the input to amplifer A is open and that all the transistors have infinite beta and no base current. The base voltage of Q8 is approximately +0.6V. The base voltage of Q21, determined by the drop across R58 and R59, is approximately +148V. This sets the emitter and collector current of Q21 to about 7 mA.

Now assume that the input of amplifier A is connected to the input amplifier (Q17). Any current sunk by the input amplifier is supplied by Q21 and Q8 through R57. Current, amplified by Q20, is coupled to Q21 through C10, and coupled to Q8 through R61. Transistors Q8 and Q20 have high voltage outputs, which increase as current through the feedback loop, R57, increases. This feedback is 180° out of phase with the input to amplifier A. Thus, the input voltage to amplifier A remains at 0V. For every milliampere of current sunk by the input amplifier, the output voltage of amplifier A rises +23.7V.

The combined voltage gain of the Voltage to Current Input Amplifier, Y-Axis and the Output Driver Amplifier A, Y Axis is about 120.

The collector current of Q8 is 7 mA, since any current through R57 into the base of emitter follower Q20 increases the voltage at the base of Q8, which is turned on sufficiently to sink 7 mA.

Diodes at amplifier A output protect against CRT arcing.

Output Driver Amplifier A, X-Axis ⓕ
Output Driver Amplifier B, X-Axis ⓖ

The operation of these circuits is identical to Output Driver Amplifiers A and B, Y Axis.

Z Multiplexer ⓘ

The Z Multiplexer, U4, selects intensity modulation voltages that represent varying intensities for scale illumination, traces, and characters displayed during digital or analog mode. The Voltage to Current Converter, Z-Axis converts the Z Multiplexer output to current sources that drive the control gate and control grid amplifiers. See Figure 8–29. The inputs to U4 are controlled by GRAT EN and L INTEN MOD.

Front panel control SCALE INTEN varies the intensity of graticule illumination. Front panel control INTEN varies the intensity of traces and characters.

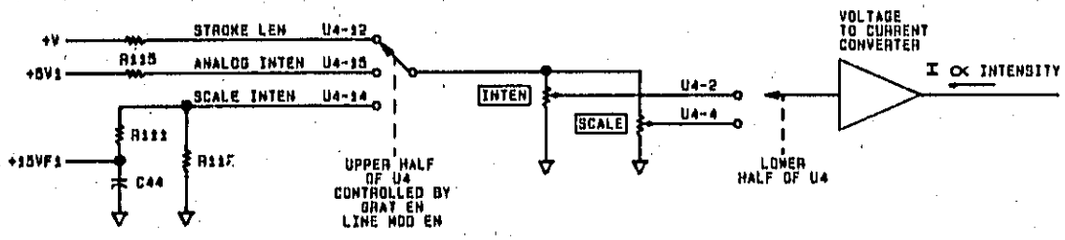


Figure 8-29. Z Multiplexer

Voltage to Current Converter, Z-Axis ❶

This circuit converts its input voltage from the Z Multiplexer to two current sinks that drive the Control Gate Amplifier and the Focus Gate Amplifier.

Common emitter amplifiers Q3 and Q13 provide one current sink; Q4 and Q14 provide the other current sink. The differential amplifier pair, Q3 and Q4, have a nominal input voltage range from 0V to +1V. CR8, R118, and R117 form a diode clamp and voltage divider so that the voltage difference to the amplifier pair never exceeds 1V.

Transistor Q13 forms a current sink inversely proportional to the intensity level. Transistor Q14 forms a current sink inversely proportional to the intensity level.

INTEN GAIN adjustment R124 controls the relative gain of the inverting and noninverting side of the amplifier.

Test point 13, at the base of emitter follower Q25, may be shorted to ground for troubleshooting. This blanks the CRT. Voltage levels noted in function block J on the schematic diagram, Figure 8-34, apply when TP13 is grounded.

Dynamic Focus, X-Axis ❽

This circuit sinks varying amounts of current from the Focus Gate Amplifier ❾ to maintain sharp focus as the X input is swept. Figure 8-30 shows that the current sink is an exponential function of the absolute value of X. Emitter current of Q40 and Q41 is a function of the voltage difference at the bases of Q40 and Q41. When X+ (TP9) is high, and X− (TP10) is low, Q40 turns on, sinking more current. When the CRT beam is at midscreen, X+ equals X−, and the voltage difference at the bases of Q40 and Q41 is zero.

Resistor R90* is a factory select part and adjusts the amount of dynamic focus compensation. Diodes CR5 and CR6 provide temperature compensation.

Focus Gate Amplifier ❾

The Focus Gate Amplifier supplies a correction voltage to the focus grid of the CRT. Figure 8-31 is a simplified schematic of the Focus Gate Amplifier. Focusing varies as front panel intensity, stroke length, and horizontal

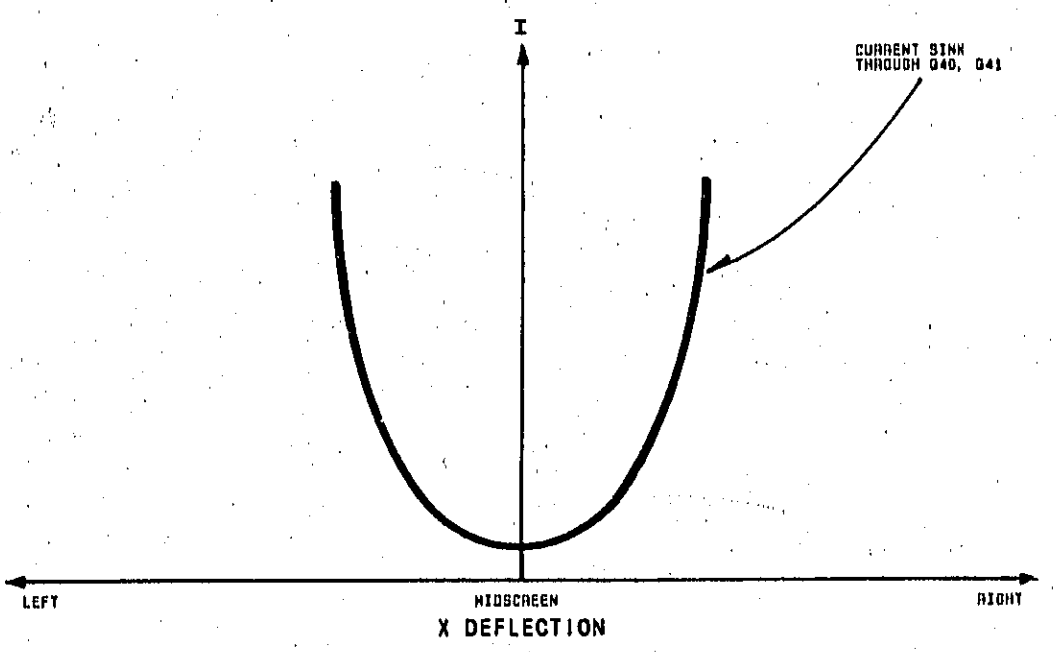


Figure 8-30. Current Source, DYN Focus

position change. Currents inversely proportional to these signals are summed at a current node; the current is amplified to produce the CONTROL GATE output. The CRT beam defocuses during graticule illumination.

The DYN FOCUS signal is a current sink proportional to the horizontal position of the CRT beam. (Refer to Figure 8-34.) When GRAT EN is high during graticule illumination, Q2 turns on and sinks DYN FOCUS current to ground; the voltage level at the base of Q11 is zero, and the beam defocuses, producing uniform graticule illumination.

When GRAT EN is low, Q2 turns off. This allows the summing of DYN FOCUS current with current from the Z Multiplexer (via Q1) that is inversely proportional to stroke length or intensity.

Transistor Q1 has low input impedance and high output impedance. It isolates the summing-current node at Q11 from the Z Multiplexer.

The correction voltage at FOCUS GATE varies from +5V to +70V.

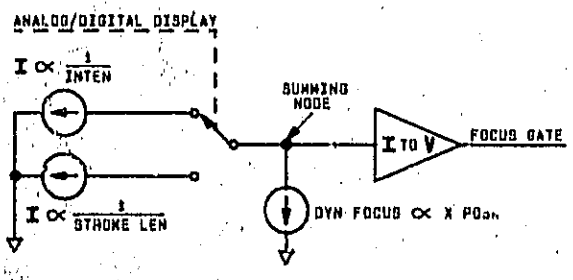


Figure 8-31. Focus Gate Amplifier, Simplified Schematic

Control Gate Amplifier (M)
Analog Blanking (K)
Analog/Digital Blanking Select (L)

The Control Gate Amplifier is a current to voltage amplifier similar to the Focus Gate Amplifier. It drives the control grid of the CRT. Beam current, proportional to stroke length or intensity, is amplified to produce the control grid voltage (CONTROL GATE) which varies from +25V to +70V. Figure 8-32 is a simplified schematic of the Control Gate Amplifier.

Blanking switch Q24 turns off the beam current according to the logic levels of analog and digital blanking signals, ANLG BLNK (TTL) and LDGTL BLNK.

In the Analog/Digital Blanking Select circuit, the ANLG/LDGTL signal (from A7) steers either L DGTL BLNK or ANLG BLNK (TTL) to pin 8 of U3. A logic high from U3 turns off Q24, shutting off current to the current to voltage amplifier. The beam is blanked; CONTROL GATE is at +25V. Diodes CR15 and CR16 ensure that no current passes to U3 when Q24 is conducting. Resistor R150 is a pull-up resistor.

The Analog Blanking circuit converts ANLG BLNK to TTL levels, for compatibility with U3. Transistor Q10 is always on, with base current of 1 mA. When ANLG BLNK is high, Q10 collector current is 3 mA and the voltage at TP12 is +4V. The CRT beam is blanked if ANLG/LDGTL is high. When ANLG BLNK is low, Q10 collector current is 1 mA and TP12 is at 0V, approximately. This blanks the CRT beam if ANLG/LDGTL is low.

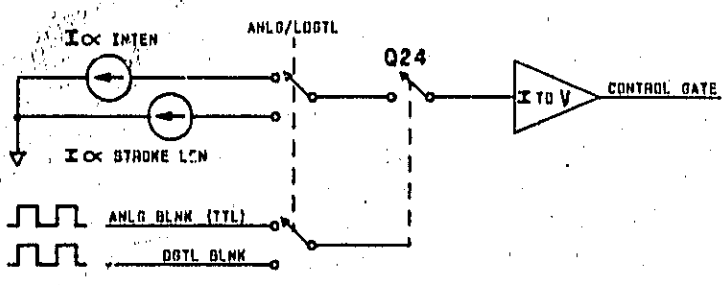


Figure 8-32. Control Gate Amplifier, Simplified Schematic

A6
XYZ AMPLIFIER ASSEMBLY
00853-60005

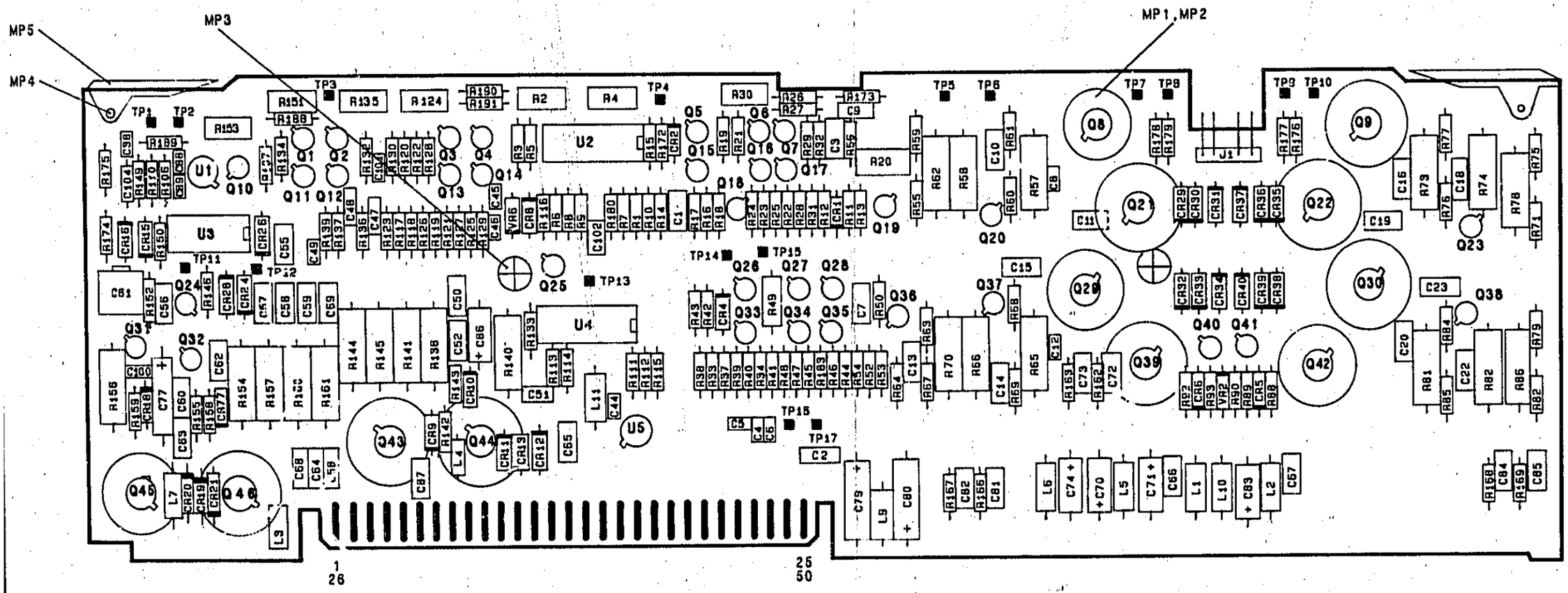
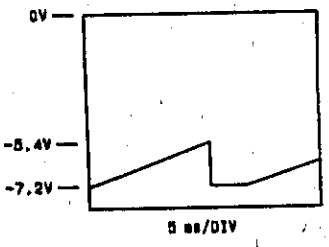
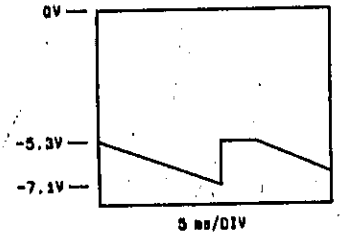


FIGURE 8-33. XYZ AMPLIFIER ASSEMBLY A6, COMPONENT LOCATIONS

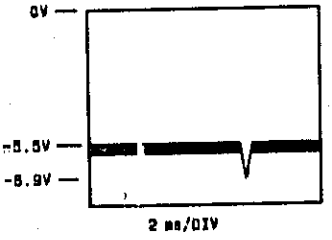
TEST POINT 17



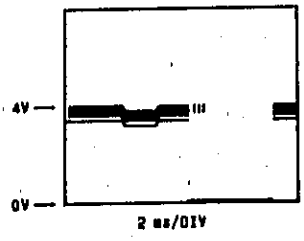
TEST POINT 16



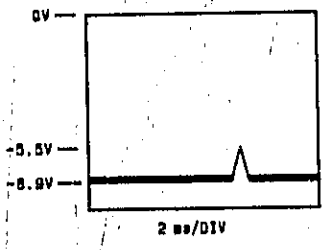
TEST POINT 15



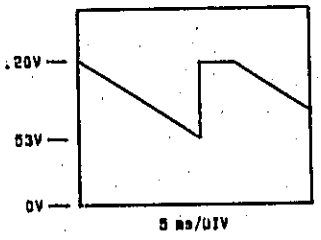
TEST POINT 11



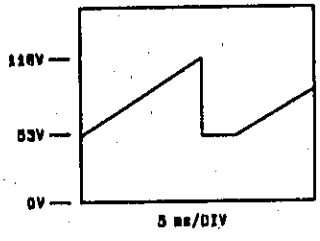
TEST POINT 14



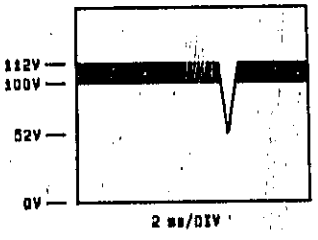
TEST POINT 10



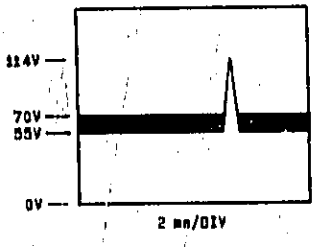
TEST POINT 9



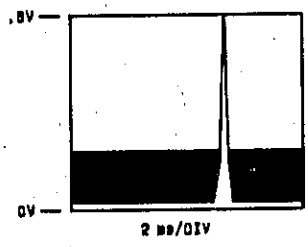
TEST POINT 8



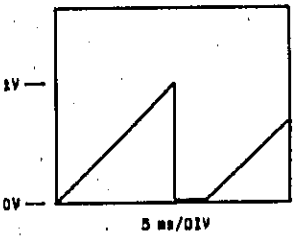
TEST POINT 7



TEST POINT 4



TEST POINT 5



SEE NOTE 7

A6 XYZ AMPLIFIER ASSEMBLY 00853-60005 (SHEET 1 OF 2)

P1

PIN	SIGNAL	TO/FROM	FUNCTION BLOCK
1 25	CTL DATE GND CONTROL GND	NOTE 8 A3P1-20,22	Q M
2 27	CTL DATE GND	NOTE 8	Q
3 29	CTL DATE GND	NOTE 8	Q
4 28	ANLG/DGTL	A7J2-39	L
5 30	NC		
6 26	NC		
7 32	L DGTL BLNK ANLG BLNK	A7J2-20 A3J1-4	L K
8 33	Z MOD	A3A1J1-6	I
9 34	SCALE INTEN FOCUS GATE	A3A1J1-9 A4P1-9,21	I H
10 35	STROKE LEN	A3P1-5	I
11 36	INTEN BRIT CH	A3A1J1-12 A7J2-34	I
12 37	L INTEN MOD	A7J2-32	I
13 38	X POSN 2	A3P1-3	C
14 39	Y POSN 1	A3P1-8	C
15 40	NC		
16 41	Y POSN	A3P1-11	B
17 42	SWEEP	A3J1-14 A3P1-44	A
18 43	DGTL Y DGTL X	A3P1-4 A3P1-22	A A
19 44	+150V +150V	A3J2-1 A3J2-1	Q Q
20 45	+150V SW +150V SW	A3J2-[3,5] A3J2-[3,5]	Q Q
21 46	+15V +15V	A3J2-8 A3J2-8	Q Q
22 47	ANLG GND ANLG GND	NOTE 8 NOTE 8	Q Q
23 48	-15V -15V	A3J2-7 A3J2-7	Q Q
24 49	NC NC		
25 50	RETURN VIDEO	NOTE 8 A3J1-15 A3P1-36	B A

Ⓖ SUPPLY FILTERING

Ⓐ DIGITAL/ANALOG SWITCH (X AND Y)

P/O A2 DISPLAY ADJUST

Ⓑ VOLTAGE TO CURRENT INPUT AMPLIFIER, Y-AXIS

Ⓒ VOLTAGE TO CURRENT INPUT AMPLIFIER, X-AXIS

P/O A2 DISPLAY ADJUST

Ⓓ OUTPUT DRIVER AMPLIFIER A, Y-AXIS

Ⓔ OUTPUT DRIVER AMPLIFIER B, Y-AXIS

Ⓕ OUTPUT DRIVER AMPLIFIER A, X-AXIS

Ⓗ OUTPUT DRIVER AMPLIFIER B, X-AXIS

Ⓘ DYNAMIC FOCUS, X-AXIS

TO CRT (VERTICAL)

TO CRT (VERTICAL)

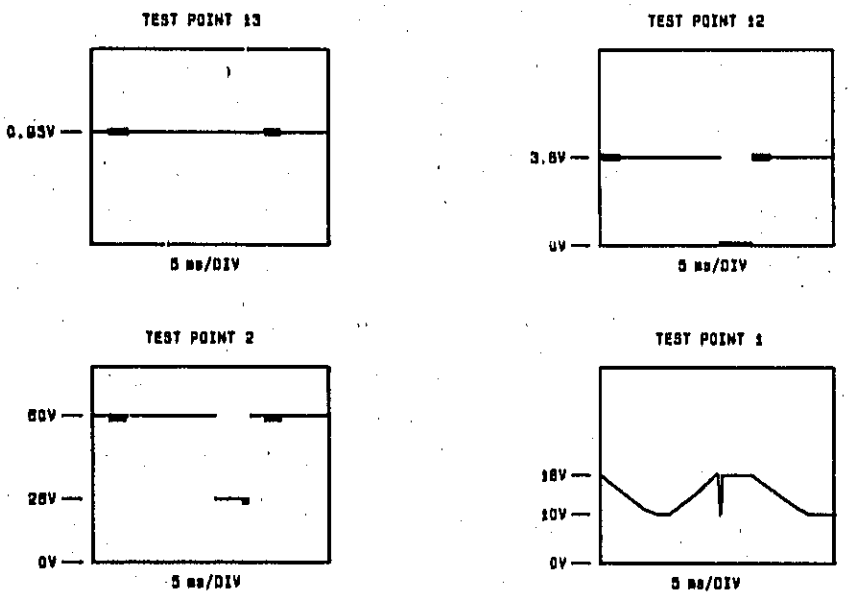
TO CRT (HORIZONTAL)

TO CRT (HORIZONTAL)

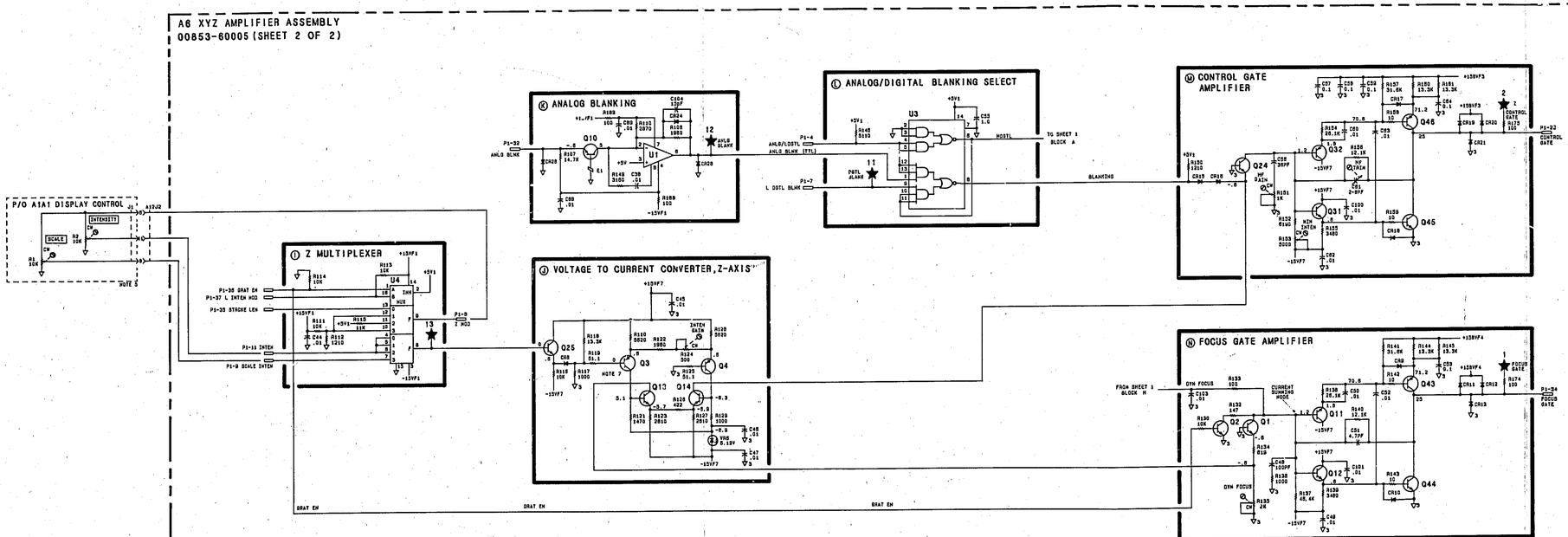
SERIAL PREFIX: 2223A

A6

FIGURE 8-34. XYZ AMPLIFIER ASSEMBLY A6, SCHEMATIC DIAGRAM (1 OF 2)


TEST POINT 13
0.65V
5 ms/DIV
TEST POINT 12
3.6V
0V
5 ms/DIV
TEST POINT 2
60V
28V
0V
5 ms/DIV
TEST POINT 1
18V
10V
0V
5 ms/DIV

SEE NOTE 7



NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. PREFIX ABBREVIATION WITH ASSEMBLY NUMBER FOR COMPLETE REFERENCE DESIGNATOR.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS (Ω). CAPACITANCE IN MICROFARADS (μF) INDUCTANCE IN MICROHENRIES (μH)
3. ASTERISK (*) DENOTES FACTORY SELECTED COMPONENT. NOMINAL VALUE IS SHOWN.
4. UNLESS OTHERWISE INDICATED, SIGNALS ENTER AT LEFT SIDE AND EXIT AT RIGHT SIDE OF FUNCTION BLOCKS.
5. SEE FIGURE 8-8 FOR CONNECTIONS.
6. MNEMONICS TABLE:

MNEMONICS	DESCRIPTION
ANLG BLNK	ANALOG BLANK
ANLG BLANK (TTL)	ANALOG BLANK IN TTL LEVELS
ANLG/L DGTL	ANALOG/LOW-DIGITAL
L DGTL BLNK	LOW DIGITAL BLANK
DYN FOCUS	DYNAMIC FOCUS
Z MOD	Z MODULATION
SCALE INTEN	SCALE INTENSITY
INTEN	INTENSITY (TRACE)
L INTEN MOD	LOW INTENSITY MODULATION
GRAT EN	GRATICULE ENABLE
X POSN 1 (2)	X POSITION 1 (2)
CTL GATE GND	CONTROL GATE GROUND
DGTL Y	DIGITAL Y
STROBE LEN	STROBE LENGTH
MODTL	HIGH DIGITAL

7. TEST POINT 11 IS SHOWN WITH SPECTRUM ANALYZER IN DIGITAL MODE. ALL OTHER TEST POINTS ARE SHOWN WITH SPECTRUM ANALYZER IN ANALOG MODE. WHEN VIEWING TEST POINTS 1, 3, 4, 5, 7-10, 12, AND 14-17, EXTERNALLY TRIGGER OSCILLOSCOPE WITH HP853A REAR PANEL BLANK (PEDESTAL) OUTPUT. SEE TABLE 8-5 FOR OTHER MEASUREMENT CONDITIONS.
   TO MAKE VOLTAGE MEASUREMENTS IN FUNCTION BLOCKS 1 THROUGH 9, FIRST PUT HP853A IN DIGITAL MODE AND THEN SET BASE TO +10.00 VDC.
   TO MAKE VOLTAGE MEASUREMENTS IN FUNCTION BLOCK L, GROUND TP13. VOLTAGES INDICATED IN VOLTS.
8. ALL GROUNDS CONNECT TO CHASSIS (GND) AT MOTHERBOARD.

SERIAL PREFIX: 2223A

A6

FIGURE 8-34. XYZ AMPLIFIER A6, SCHEMATIC DIAGRAM (2 OF 2)

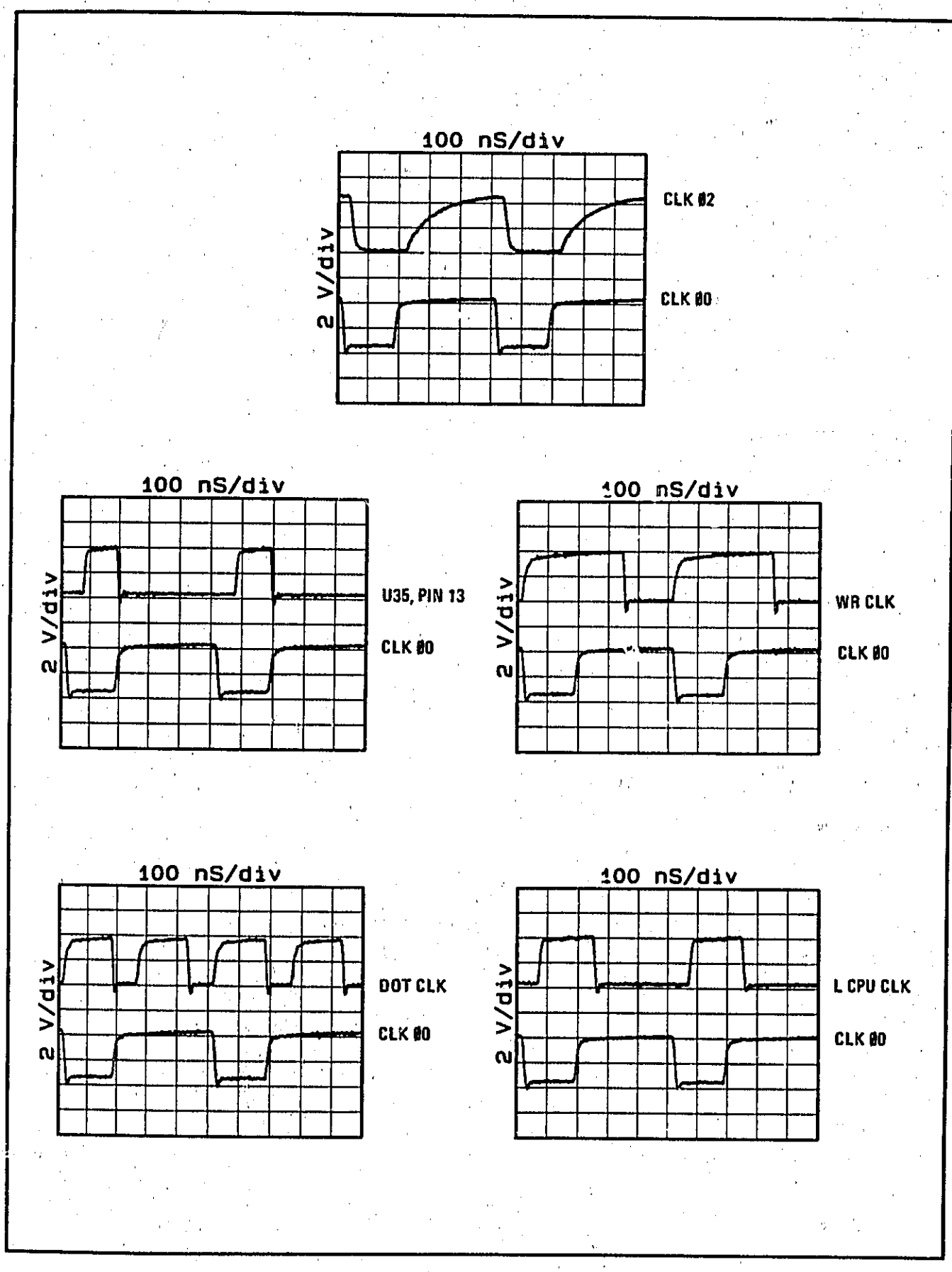


Figure 8-35, Processor Clocks Referenced to CLK Ø0

PROCESSOR ASSEMBLY A7, CIRCUIT DESCRIPTION

The Processor Assembly controls the HP 853A mainframe, which consists of two functional systems: the Input System and the Output System. (See General Circuit Description and Figure 8-5.) The central processing unit (CPU) and counter control these systems:

- The CPU controls conversion of sweep, video, and front-panel signals to digital data, and stores it in memory.
- The counter converts digital data to analog information and displays it on the CRT.

CPU and Program ROM Ⓐ

The CPU, U50, manipulates data using the address bus, A0 through A15, and the data bus D0 through D15. (Refer to Data Multiplexer.) The address bus specifies the hardware or memory location that is to supply or receive data on the data bus. The CPU stores data in Stroke Memory or System Memory Ⓕ Ⓒ . It also fetches data from Stroke and System memory, and the Program ROM Ⓐ, U34, which is a read-only memory that contains instructions for the CPU.

This circuit has the following control lines.

L ROM EN (low ROM enable) switches the multiplexers in System Memory and Stroke Memory. When L ROM EN is high, the CPU address bus addresses memory. The CPU Program ROM is disabled and the CPU controls the data on the data bus, D0 through D15. When L ROM EN is low, the counter bus addresses memory and controls the data on the data bus, D0 through D15. While the Counter controls the data bus, the Program ROM is enabled, and the CPU fetches a command for its own internal operation, using the CPU data bus lines d0 through d7.

LR/W (low-read/write) and **R/LW** (read/low-write). LR/W determines the direction of data through the Data Multiplexer Ⓑ . When LR/W is low, data passes from the Data Multiplexer to the CPU. LR/W and R/LW control HP-IB data flow through U24, in the HP-IB Interface and Sweep Status Interface Ⓛ.

L CPU RESET (low CPU reset) restores the CPU to its initial state. When power is initially turned on, comparators U53A and U53B generate the L CPU RESET pulse, which remains low until the +5V supply exceeds about +4V. Capacitor, C1,and R3 cause a delay which holds the voltage at pin 1 of U53 low for about 200 ms. The L CPU RESET pulse may also be generated by grounding TP5.

All clocks are 2 MHz, except DOT CLK, which is 4 MHz. Figure 8-35 shows clock waveforms, all referenced to CLK (Ø0).

Data Multiplexer Ⓑ

The CPU processes eight bits of data at a time. The data multiplexer converts the 8-bit CPU data bus, d7 through d0, to a 16-bit data bus, D15 through D0. Table 8-6 shows how the busses correlate.

When accessing System Memory, the CPU processes data on data lines D7 – D0 through transceiver U20.

When accessing Stroke Memory, the CPU processes data on data lines D15 – D0 through transceivers U20, U21, and U22. The CPU processes Stroke Memory in three steps:

First, U20 is enabled, and eight bits, D15 – D8, which correspond to CPU data bits d7 – d0, are processed.

Second, U21 is enabled, and four bits, D7 – D4, which correspond to CPU data bits d7 – d4, are processed. The CPU ignores CPU data bits d3 – d0.

Third, U22 is enabled, and four bits, D3 – D0 which correspond to CPU data bits d7 – d4, are processed. Again, the CPU ignores CPU data bits d3 – d0.

Table 8-6. 8-Bit CPU Data Bus and 16-Bit Data Bus Correlation

8-Bit CPU Data Bus	Translates to 16-Bit Data Bus	System Memory Data Contents	Stroke Memory Data Contents
d7–d0	D15–D8	Character Buffers, CPU Scratch Pad & Stack	8 MSB Stroke Data
d7–d4	D7–D4	Not Used	4 LSB Stroke Data
d7–d4	D3–D0	Not Used	Blanking Data

Control lines from U15, U57B, and U57D enable tranceivers U20, U21, and U22. When L ROM EN is high, and pins 4 and 5 of U15 are low, U15 is enabled. A10 and A11 determine which U15 output is active (low).

Stroke Memory and Multiplexer

Stroke Memory contains four static read/write, random access memory (RAM) chips, U8, U9, U10, and U11 that receive and send data on the data bus. These RAMs are accessed by a 10-bit address, AD0 – AD9. Multiplexers U40, U41, and U42 route commands from the CPU, Counter, and Memory and I/O Select Generator to these RAMs.

Stroke data is stored in stroke memory as 1024 16-bit words. There are 512 words for trace A and 512 words for trace B. These words correspond to 512 positions on the CRT display, located across the CRT's horizontal axis. A 16-bit word is processed as one 8-bit byte and two 4-bit nibbles. Table 8-7 lists the contents of Stroke Memory.

The high byte of stroke data, D15 – D8, contains the 8 most significant bits representing the vertical value of the video signal. The low byte of stroke data, D7 – D6, contains the two least significant bits of the vertical value. D4 – D3 are blanking information. Bits D1 and D0 are not used. The extreme right and left positions on the CRT's horizontal axis are blanked so that only trace data within the graticule area is displayed. Bits D5 and D4 are fractional bits (1/2 bit and 1/4 bit) used for digital averaging; they are not displayed.

L ROM EN determines whether the CPU or Counter is addressing the RAMs. The CPU addresses the RAMs with address bus bits A0 – A9. The CPU stores stroke data in Stroke Memory sequentially. It also fetches data from Stroke Memory for arithmetic operations, such as normalizer functions.

The Counter addresses the RAMs with counter bus bits CNT5 – CNT13, and CNT15. As the Counter counts, stroke data is accessed sequentially for display on the CRT. CNT15 selects trace A or trace B.

The following signals control Stroke Memory:

L ROM EN (low ROM enable) switches multiplexers U40, U41, and U42. When L ROM EN is low, the A inputs are selected. When L ROM EN is high, the B inputs are selected (SEL B).

L CS (low chip select) is the enabling input to the RAM chips U8, U9, U10, and U11. Multiplexer U40 selects either L MS1 or L MS3 to be the low chip select signal. When L CS is low, Stroke Memory is enabled.

MS1 (memory select 1) enables the Stroke Memory RAMs (via L CS). When L ROM EN is high and MS1 is low, the CPU controls Stroke Memory.

MS3 (memory select 3) enables the Stroke Memory RAMs (via L CS). When MS3 is low and L ROM EN is low, the Counter controls stroke memory.

HI-BYTE R/LW (high byte read/low-write) controls the direction of data in U8 and U9.

LO-BYTE R/LW (low byte read/low-write) controls data direction in U10.

Table 8-7. Processor Addresses

CPU Address	Function
	General I/O Interfaces
$0	Analog-to-Digital Converter (Low Byte)
$8	Analog-to-Digital Converter (High Byte)
$20	Display Pushbuttons, Write Control
$28	Display Pushbuttons, Store Control
$30	HP-IB Address Switch, Sweep Status
	Control Latch Interface
$19	Trigger Sweep Start/Reset Function
$18	Arm the Sweep Start/Reset Function
$1A	End Request Conversion Pulse
$1B	Start Request Conversion Pulse
$1C	Input Select A Low
$1D	Input Select A High
$1E	Input Select B Low
$1F	Input Select B High
$12	Disable Analog Fast Sweep Function
$13	Enable Analog Fast Sweep Function
	HP-IB Registers
$38	HP-IB Data Register
$39	Interrupt Status Register for Incoming Data
$3A	Interrupt Status Register for Bus Handshake
$3B	Serial Poll Register
$3C	HP-IB Address Status Register
$3D	Auxiliary Command Register
$3E	HP-IB Switch Selected Address Register
$3F	Not Used
	System Memory
$380–3BF	Character Buffer for Upper Printed Line on Display
$3C0–$3FF	Character Buffer for Lower Printed Line on Display
$40–$37F	Scratchpad Memory and Machine Stack for CPU
	Stroke Memory
$400–$5FF	Blanking Data for Trace B
$600–$7FF	Blanking Data for Trace A
$800–$9FF	Stroke Data for Trace B (High Byte)
$A00–$BFF	Stroke Data for Trace A (High Byte)
$C00–$DFF	Stroke Data for Trace B (Low Byte)
$E00–$FFF	Stroke Data for Trace A (Low Byte)
$1000–DFFF	Not Used
	Program Memory (ROM)
$E000–$FFFF	HP-IB and Plot Subroutines Control Setting Display Subroutines Executive Program and Trace Data Handling Initialization and Test Subroutines

CTL R/LW (control read/low-write) controls data direction in U11.

System Memory and Multiplexer ⓕ

System Memory is similar in structure to Stroke Memory. System Memory comprises static RAM chips, U6 and U7, and multiplexer chips, U37 – 39. The multiplexers route signals from the CPU, Counter, and Memory and I/O Select to the RAMs.

The RAM chips contain a scratch pad memory and machine stack for the CPU's own internal operation. They also contain two character buffers, one for each line of character display. Refer to Table 8-7.

L ROM EN, as in Stroke Memory, determines whether the CPU or Counter is addressing RAM. By addressing RAM with address bus lines A0 – A9, the CPU stores the front panel settings in the character buffers as ASCII code. Counter bus lines CNT9 through CNT14 select the character position, and CNT5 selects the upper or lower buffer.

The following signals control System Memory:

L ROM EN (low ROM enable) switches the multiplexers, U37, U38, and U39. When L ROM EN is high, the B inputs are selected (SEL B) When L ROM EN is low, the A inputs are selected.

L CS (low chip select) is the enabling input to the RAM chips U6 and U7. Multiplexer, U39, selects either MS0 or MS2 to be the low chip select signal. When L CS is low, System Memory is enabled.

MS0 (memory select 0) enables System Memory RAMs (via L CS). When MS0 is low and L ROM EN is high, the CPU controls System Memory.

MS2 (memory select 2) enables the System Memory RAMs (via L CS). When MS2 and L ROM EN are low, the Counter controls System Memory.

SYS R/LW (system read/low-write) controls direction of data flow in System Memory.

Memory and I/O Select ⓔ

This circuitry generates the following control lines.

MS0 Refer to System Memory and Multiplexer ⓕ.

MS1 Refer to Stroke Memory and Multiplexer Ⓖ.

MS2 Refer to System Memory and Multiplexer ⓕ.

MS3 Refer to Stroke Memory and Multiplexer Ⓖ.

L I/O SEL (low input/output select), when low, enables the I/O Decoder.

DSPL TRACE and **DSPL CHAR** together control the timing and direction of the DGTL X ramp.

DSPL TRACE (display trace) controls timing of the negative portion of the DGTL X ramp for display of traces. It also initiates strobing of stroke data to Y Data Buffer. DSPL TRACE is high when traces are displayed. (Refer to circuit descriptions of Display Control Logic and Blanking Logic in this section. Also refer to Digital X Generator in A5.)

DSPL CHAR (display characters) controls timing of the positive portion of the DGTL X ramp for display of characters. It enables blanking logic for characters, and provides phase shift in Counter. (Refer to Display Control Logic, Blanking Logic, and Counter circuit descriptions. Also refer to Digital X Generator in A5.)

Stroke Select Generator ❶

STROKE SEL determines which of the Y Data Buffer (A5) inputs and outputs are enabled.

Display Control Logic ❽

This circuit generates signals that time the display of information on the CRT. It controls some circuitry on the Data Converter Assembly, A5.

STRK GEN TIMG (stroke generator timing) controls the timing of the Digital Y Generator (A5) and Blanking Logic. It times the drawing and blanking of trace data from Stroke Memory (A7) that is stored temporarily in the Y Data Buffer (A5). When STRK GEN TIMG is high (6 μs), the Digital Y Generator (A5) processes stroke information from the Y Data Buffer and generates DGTL Y; a stroke is drawn which corresponds to one of the 512 buckets of the CRT display. When STRK GEN TIMG is low (1 μs), the CRT beam is blanked (L DGTL BLNK) and the Y Data Buffer is switched. See Figure 8-36 and Data Converter Assembly A5 circuit description.

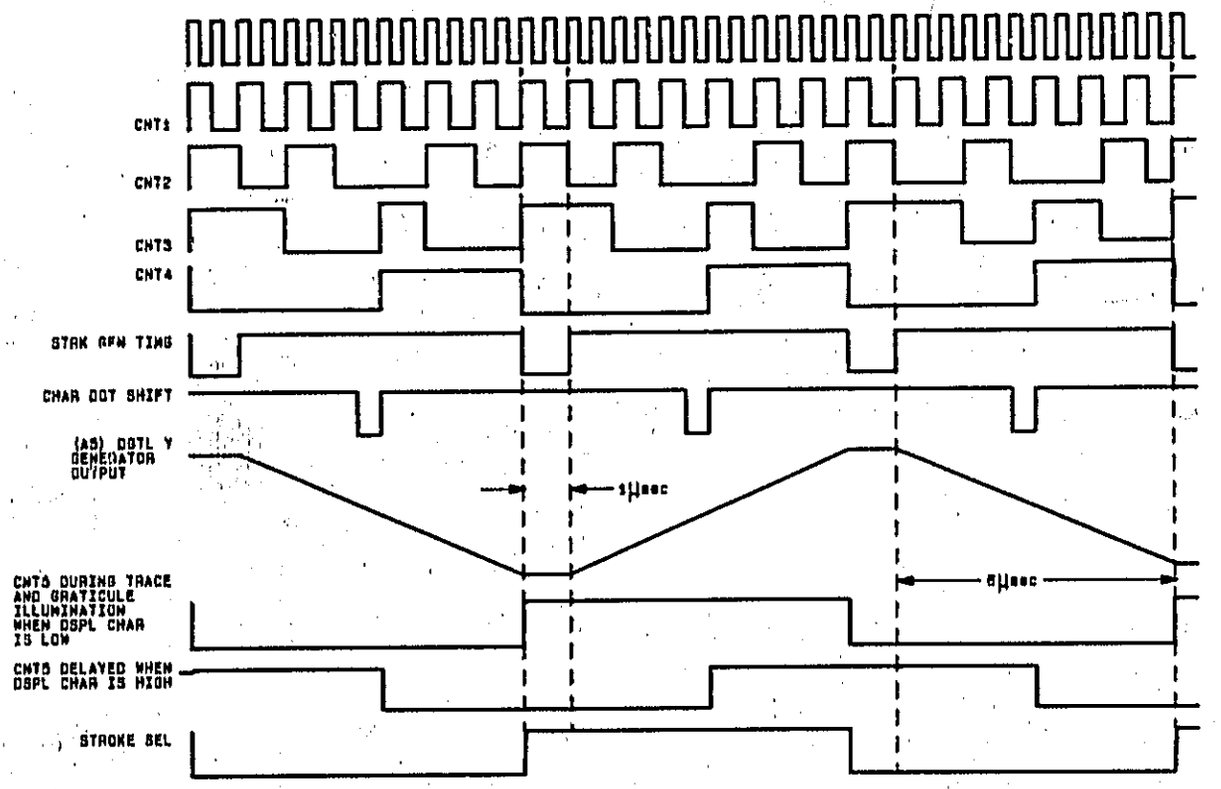


Figure 8-36. Stroke Generator Timing

DSPL TRACE (display traces), when high, enables STRK DATA STRB.

STRK DATA STRB (stroke data strobe) strobes trace data into the Y Data Buffer (A5). Refer to Data Converter A5 circuit description.

STROKE BLNK (stroke blank) blanks the CRT as the Y DATA buffer (A5) is loaded.

Refer to Data Converter circuit description.

DSPL CHAR (display characters) is high during character display.

L X CLAMP R (low X clamp right) clamps DGTL X sweep ramp (A5) to 1V.

X HOLD LEFT (X hold left) is active during mixed mode. This signal holds DGTL X value constant (A5) during analog display interval, so that character line is positioned correctly and all characters are displayed. (Refer to Counter circuit description for detailed operation of mixed mode.)

Read/Write Select ⓒ

READ/WRITE SELECT generates four commands for stroke and system memory. These outputs are active one at a time when A15 and WR CLK are low and LR/W is high. A10 and A11 determine which output is active.

SYS R/LW (system read/low-write) controls the direction of data in System Memory.

CTL R/LW (control read/low-write) controls data direction in the portion of Stroke Memory that corresponds to data lines D0 through D3.

LO – BYTE R/LW (low-byte read/low-write) controls data direction in the portion of Stroke Memory that stores the least significant data bits of the VIDEO (Y) data.

HI-BYTE R/LW (high-byte read/low-write) controls data direction in the portion of Stroke Memory that stores the eight most significant data bits of the video data.

Counter ⓓ

The counter fetches trace and character data from System Memory and displays it, together with graticule illumination, on the CRT. It addresses System Memory via the counter bus, CNT1 – CNT16, and controls the data bus when L ROM EN is high.

CNT1 through CNT4 determine that strokes are drawn every 7 μs. CNT5 through CNT13 determine that a trace is drawn in 3.58 ms and consists of 512 strokes (481 within the graticule). CNT14 through CNT16 select what is being drawn during the display refresh cycle: trace A, trace B, characters, or graticule illumination. The display refresh cycle, shown on Figure 8-37, repeats every 17.9 ms (55.8 Hz).

CNT5 is delayed when it selects either the upper or lower row of characters for display. When DSPL CHAR is high, it is gated with CNT4 at U54B, delaying CNT 5. See Figure 8-36.

CNT1 through CNT16 are produced by dividing L CPU CLK. The first divider in the chain, U36, divides 2 MHz by 14 to produce CNT1 through CNT4. U27 divides CNT4 by 256, and the first stage of U48A divides the U27 output by 2, producing CNT5 through CNT13. The remainder of U48A is a divide by 5, producing C14 through C16.

At sweep speeds 5 msec/DIV or faster (10 ms/DIV or faster if in DGTL AVG mode), the CPU does not have enough time to process the analog SWEEP and VIDEO signals into digital information for display on the CRT. To maintain display information, analog traces and digitally controlled characters and graticule illumination are displayed alternately on the CRT. This is called mixed mode. The Interface Assembly, A9, monitors the plug-in sweep speeds and signals when the sweep speeds are greater than or equal to 5 ms/DIV (or 10 ms/DIV); SLOW SWP goes low.

The CPU reads the sweep status interface portion of U12 (L) at the end of a sweep. When SLOW SWP goes low, it initiates the mixed mode process: ANLG FST SWP EN goes high (CPU address Δ13). The Counter gates ANLG FST SWP EN with RETRACE, producing ANLG FST SWP, which goes to Blanking Logic ⓚ, producing ANLG/LDGTL. ANLG/LDGTL travels to XYZ Amplifier Assembly A5, and ultimately produces the signal HDGTL that switches the Digital/Analog Switch (A6), which selects either the plug-in VIDEO and SWEEP signals, or the DGTL X and DGTL Y signals, to drive the CRT deflection plates.

Both of the digitally derived traces are blanked (but not cleared) during mixed mode operation (L DGTL BLNK). The Counter cycles through its normal display sequence: trace A (blanked), graticule illumination,

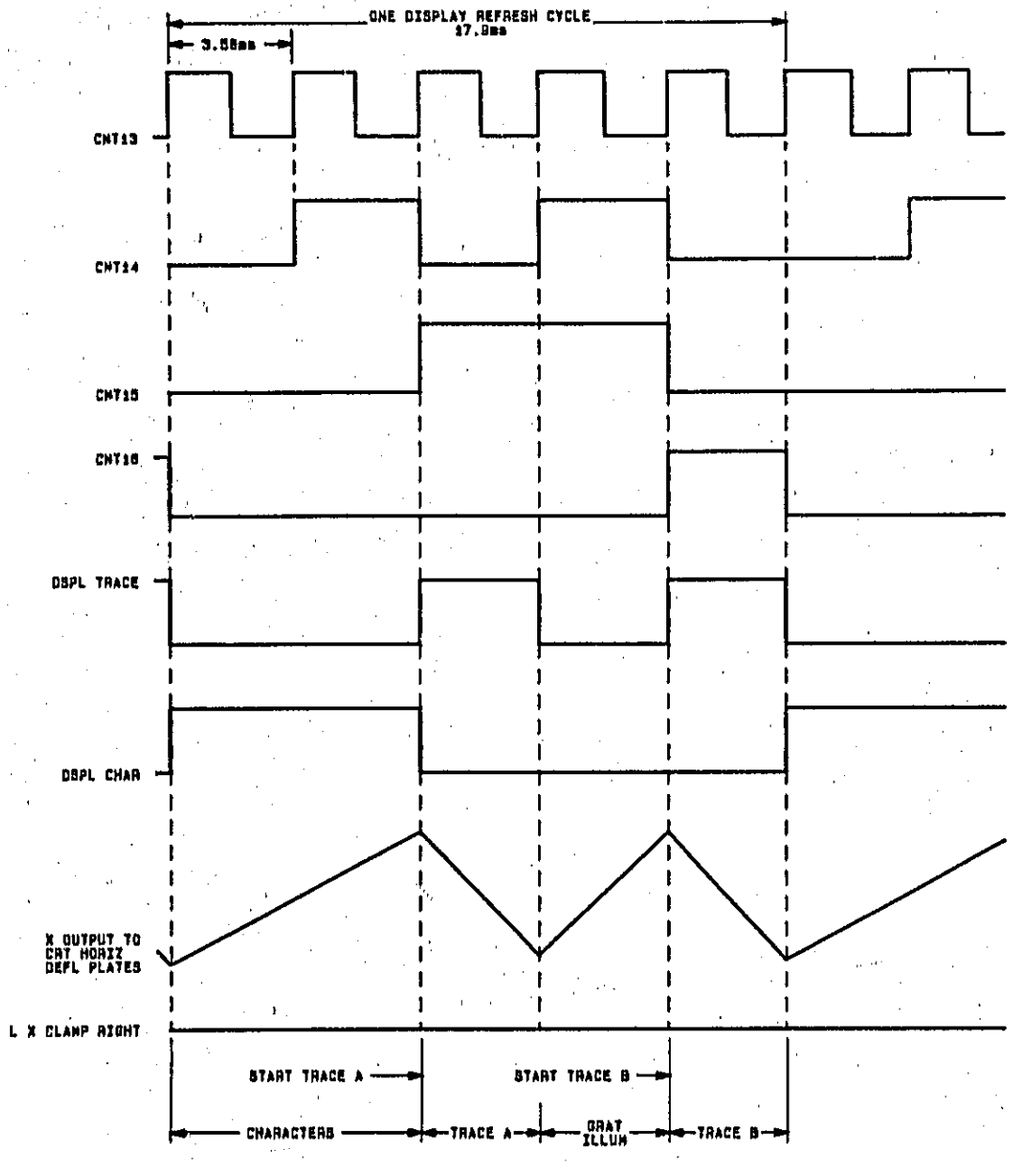


Figure 8-37. Display Refresh Cycle

trace B (blanked), and characters; except that trace B timing (trace B is now analog) is controlled by RETRACE instead of DGTL X.

Figure 8-38 shows how trace B timing is controlled in mixed mode. After graticules are drawn, COUNT EN goes low. Normally, COUNT EN would remain low for 1 μs, but since the mainframe is in mixed mode, COUNT EN does not go high again, enabling the Counter to count, until RETRACE signals the start of the plug–in sweep, by going low. The Counter now counts for 3.58 ms, and after this period, COUNT EN again goes low, this time waiting for the end of the plug-in sweep, which is signalled by RETRACE going high.

I/O Decoder Ⓜ

The CPU uses the I/O Decoder to enable, one at a time, various interfaces and latches that receive or send data according to CPU commands. The I/O Decoder is enabled when L ROM EN is high and I/O Sel is low. Address bus lines A3, A4, and A5 determine which interface, latch, or command is enabled.

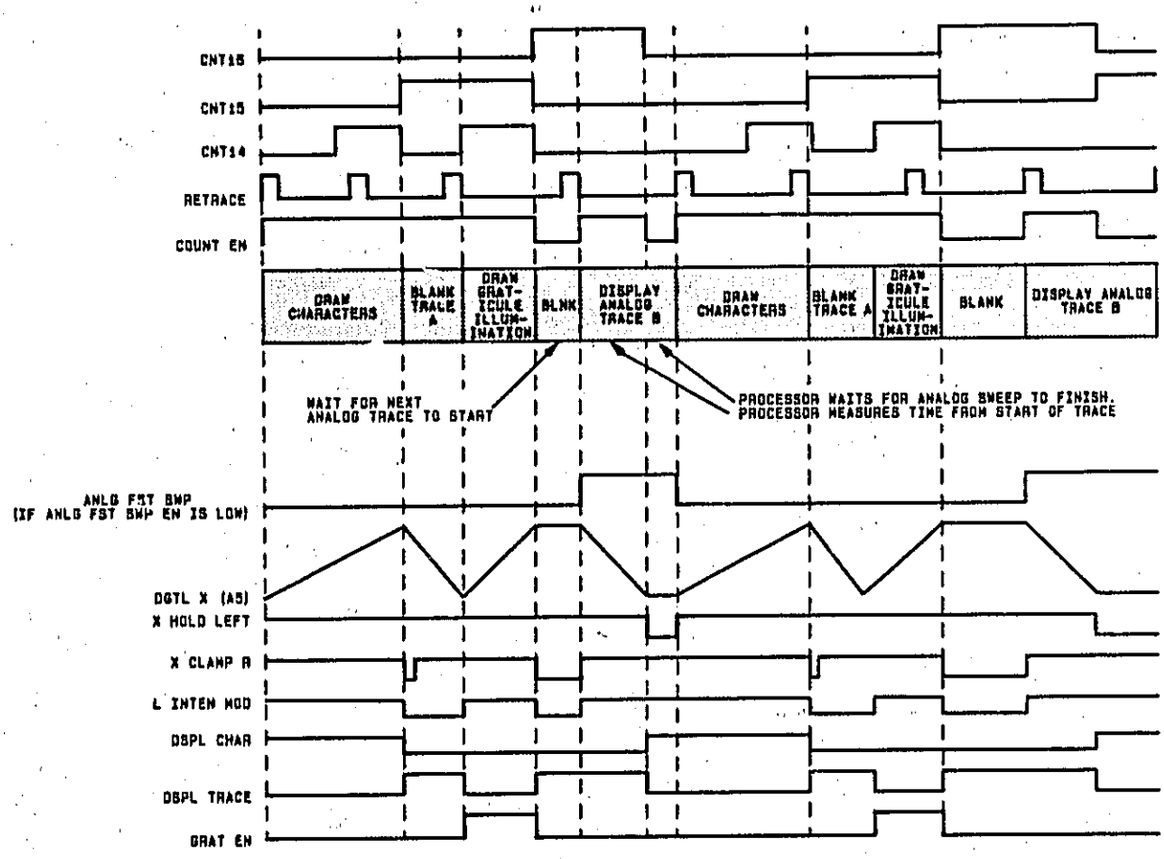


Figure 8-38. Mixed Mode Timing (Analog/Digital Display)

The I/O Decoder also enables commands for Data Converter Assembly A5.

Table 8-8 lists the circuitry controlled by the I/O Decoder.

Table 8-8. I/O Decoder Truth Table

A5	A4	A3	CPU Addresses	I/O Decoder Output Enabled
1	1	1	$38-3F	HP-IB Talk & Listen Interface (L)
1	1	0	$30-37	HP-IB Address Switch & Sweep Status Interface (L)
1	0	1	$28-2F	Store Control Switch (O)
1	0	0	$20-27	Write Control Switch (P)
0	1	1	$18-1F	Control Latches (N)
0	1	0	$10-17	Control Latches (N)
0	0	1	$8-F	ADC HI BYTE (M)
0	0	0	$0-7	ADC LO BYTE (M)

HP-IB Interface and Sweep Status Interface (L)

The microprocessor-controlled device, U24, handles all the talk and listen functions that occur during HP-IB operation. During HP-IB operation, the CPU sends and receives data (D8 – D15), using address bus lines A0, A1, and A2, which correspond to address locations $38 through $3F. U24 formats the data to and from the HP-IB device. U23 and U14 are buffers. (Refer to Table 8-7.)

R/LW and **L/RW** dictate whether the CPU is reading or writing to the HP-IB device.

Buffer U12 is enabled when the I/O Decoder is enabled and the CPU is accessing address $30. The HP-IB address is sensed by U12. The rear panel ADDRESS switch provides contact closures to ground, which are translated to TTL levels with pull-up resistors.

Buffer U12 also stores plug-in sweep status information.

When LMANUAL is low, it indicates that the sweep is in manual mode.

When SLOW SWP is high, it indicates that the sweep is slow enough to digitize. (Refer to Counter ⓓ.)

When RETRACE is high, it indicates that the plug-in is retracing.

Store Control Switch ⓞ

This interface buffers four inputs from the front panel pushbuttons that control the CRT display. The inputs are contact closure to ground, translated to TTL input levels by pull-up resistors. The CPU accesses U4 at address $28, when the I/O Decoder is enabled.

U4 also buffers inputs from Data Converter Assembly A5.

ADC BUSY (analog to digital conversion busy)is high during analog to digital conversion and goes low when conversion is finished.

LNOISE is low when the VIDEO input (A5) has noise characteristics.

Write Control Switch ⓟ

This interface buffers six inputs from the front panel pushbutton switches that control the CRT display. These inputs, again, are contact closure to ground and are translated to TTL input levels by pull-up resistors. The CPU accesses buffer U3 at address $20 when the I/O Decoder is enabled.

Control Latches ⓝ

The CPU uses the control latches to control various operations of Data Converter Assembly A5 and the plug-in. Address lines A1-A3 specify which latch output is active (high) and A0 determines whether the latch is set or cleared. (Refer to Table 8-7.)

The following signals are control latch outputs:

REQ CONV (request conversion) initiates the analog to digital conversion in Data Converter Assembly A5.

IN SEL A and **IN SEL B** (input select A and input select B) select analog signals for digital conversion. (Refer to Table 8-5 and A5 circuit description.)

L SWP TRIG (low sweep trigger) triggers a sweep in the plug-in when a high from U30 pin 9 is ORed with TRIG from U24.

ANLG FST SWP EN (analog fast sweep enable) enables mixed mode. (Refer to Counter ⓓ.)

Blanking Logic ⓚ

Blanking Logic decodes timing signals and switch positions to turn off the beam on the CRT.

The signal at TP4 (L DGTL BLNK) blanks the beam of the CRT during digital display mode. When the signal at TP4 is low, the CRT is blanked. During analog display mode, the blanking signal from the plug-in blanks the CRT beam.

ANLG FST SWP EN (analog fast sweep enable), when high, blanks digital traces and enables mixed mode. (Refer to Counter circuit description in this section.)

STRKE GEN TIMG (stroke generator timing), when low, blanks for 1 μs, each 7 μs.

STRK BLNK LCHD (stroke blank latched), when low, blanks digitally displayed strokes.

WACTL and **WBCTL** (write A control and write B control), when low, blank digital trace A and digital trace B, respectively.

L CHAR DOTS (low character dots) controls blanking of the raster for character display. Character dots are drawn when the signal is low.

ANLG FST SWP is a timing signal for mixed mode. (Refer to Counter circuit description in this section.)

ANLG/LDGTL (analog/low-digital) selects digital or analog display. When low, digital display is active; when high, analog display is active.

Character Generator ❶

The Character Generator generates two rows of characters onto the CRT by drawing a dot matrix on a vertical raster. The Counter forms the raster, which is a series of ramps, by alternately fetching the two Y Data Buffer outputs that correspond to the endpoints of the ramps. As the ramps are drawn, the character generator blanks portions of the raster. The portions not blanked form up to eight dots on each positive-going ramp, as shown on Figure 8-39.

The CPU senses the front panel control settings and stores them as ASCII code in System Memory. (ASCII is the American Standard Code for Information Interchange.) During the character portion of the display refresh

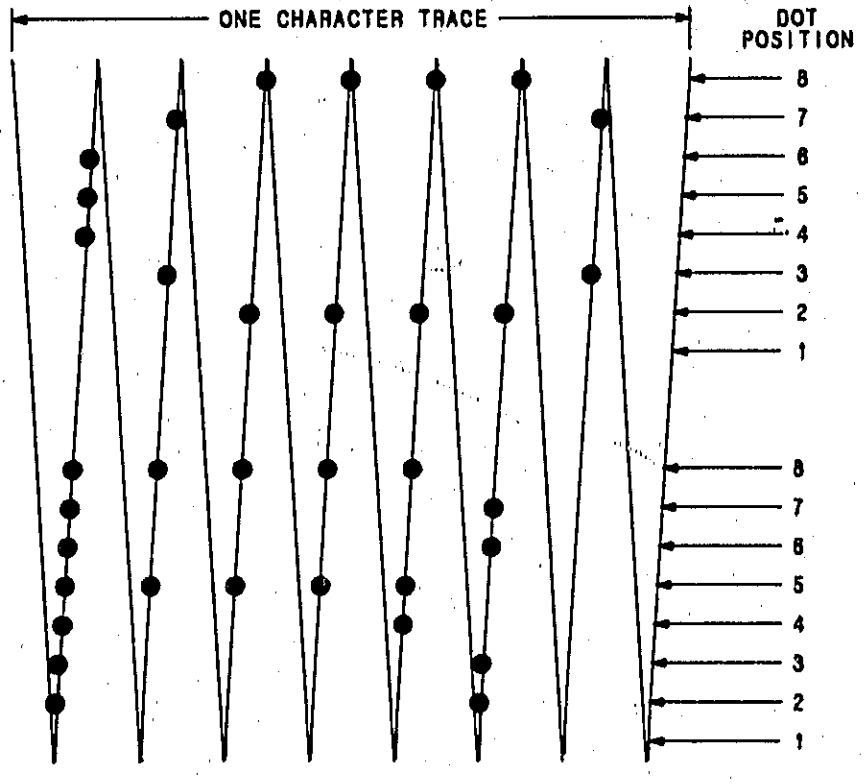


Figure 8-39. Dot Matrix Blanking Superimposed on Raster

cycle, the Counter stores the ASCII code in buffer U19. The code, together with CNT6, CNT7, and CNT8 form the address to the character ROM, U33.

The dot matrix output from U33 is the input to both U31 and U32 shift registers. U31 and U32 shift out the dot positions. A dot represents a portion of the vertical raster which is not blanked, and is 250 ns wide.

Refer to timing diagram, Figure 8-40, for the following cycle.

CHAR DOT SH goes high. Character code (ASCII) from address $3C2 in System Memory is clocked into buffer U19 one or more times by CLK Ø0 gated with A15 (ROM EN), and passes to character ROM U33.

CHAR DOT SH goes low. Dot positions for the letter "R" are loaded into shift registers U31 and U32.

DOT CLK EN inhibits the shifting of dot positions out of U31 and U32. When DOT CLK EN goes low, dots for "R" are shifted out. The most significant bit of U32, H, is shifted out first. Bit H, and also bits G, F, and E which follow, are grounded. Thus, L CHAR DOT, the output at pin 7, is initially high and these dot positions are blanked. Next, bits D, C, B, and A of U32 are shifted out. These bits are high and cause L CHAR DOT to go low. L CHAR DOT remains low as bits H, G, F, and E shift out of U31, as these bits are also high for the letter "R." This produces a pattern of dots on the CRT that form the left edge of "R."

While dot positions for "R" shift out of U32 and U31, ASCII code for "C"(address $382) is loaded into buffer U19. After the last bit for "R"(bit E of U31) shifts out, CHAR DOT SH goes low, and dot positions for "C" are transferred from U19 into U31 and U32. Now, dot positions for "C" shift out. Bits H through A of U32 and H through C of U31 shift out, forming the L CHAR DOT signal which produces, this time, a pattern of dots on the CRT that form the left edge of the letter "C."

Note that L CHAR DOTS on Figure 8-40 corresponds to the left edges of "R" and "C" drawn on the first positive ramp in Figure 8-39.

The preceding sequence occurs eight times for each pair of characters, upper and lower, shifting to the next character column with each new cycle. One sweep contains two rows of sixty-four characters. Only sixty are accessible by the user. Each row of character spaces is sequentially numbered from left to right.

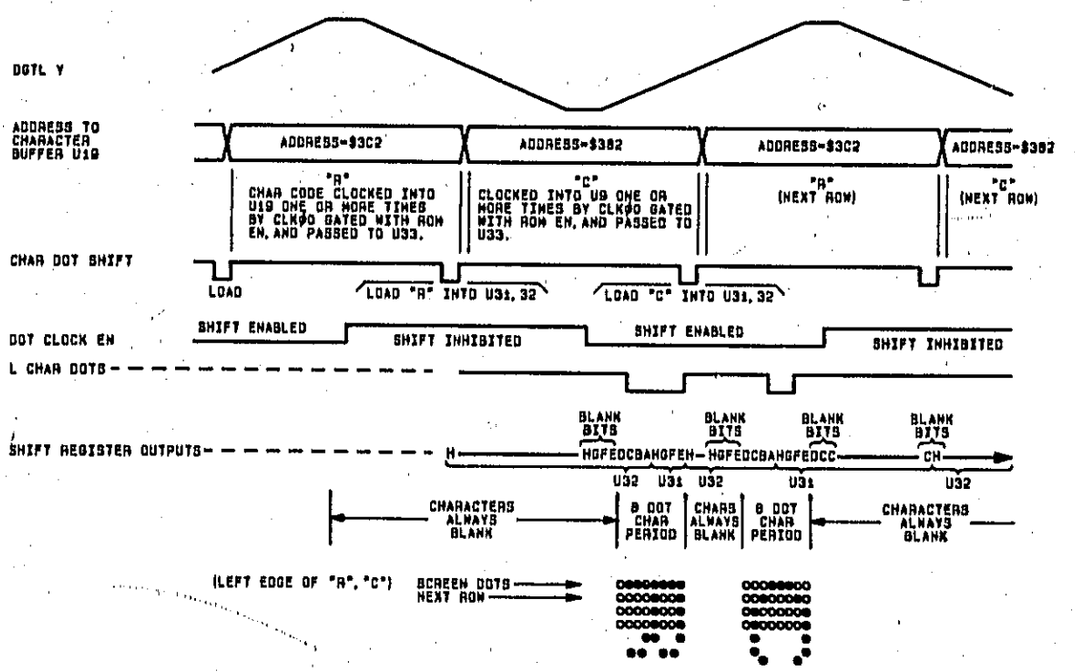


Figure 8-40. Character Generator Timing

CNT 5 chooses the upper or lower row of characters for display. (For proper character display, CNT 5 is delayed by the Counter circuitry when DSPL CHAR is high. See Figure 8-36.)

L CHAR DOT (low character dots) is high when the trace is blanked, and is low when a character dot is being drawn.

STROKE SEL (stroke select) selects odd or even strokes. It selects one of the Y Data Buffer outputs.

DOT CLK EN (dot clock enable), when high, inhibits the shift register output. It is the STROKE SEL signal, delayed by one CLK Ø0 cycle.

DOT CLK clocks the shifting of dot positions (bits H through A).

CHAR DOT SH (character dot shift) enables the shift registers, U31 and U32.

TROUBLESHOOTING

Troubleshoot Processor Assembly A7 using the signature analysis troubleshooting diagrams, Figure 8-41. These diagrams supply instructions for verifying operation of most of the digital circuitry on Processor Assembly A7.

The procedure first checks clock circuitry, then checks the address bus, address decoding circuitry, the counter and counter bus (checks A – E). If this circuitry is operating correctly, the data bus and character generator can be verified next (checks F and H). The I/O buffers can also be verified (check I).

The above procedure does not fully test stroke and system memory (U6 – U11) or HP-IB circuitry (U14, U23, U24).

A system memory check and stroke memory check is activated when the HP 853A is turned on. This self test can be activated manually. Digital test routines #7 – #9, described in Section V, identify faulty memory components with fault location indicators displayed on the CRT. (Refer to Table 5-5.)

Signature Analysis also locates program ROM (U34) and character ROM (U33) failures.

Troubleshoot the HP-IB interface circuitry using signature analysis and digital storage test routine #A. First, use signature analysis to verify all input lines to the HP-IB microprocessor, U24. Then, activate digital storage test routine #A (refer to Section V). Test routine #A checks U24, setting U24 to a talk-only, listen-only mode for self-test. When test routine #A is active, U24 ignores any signals from the HP-IB device. Replace U24 if the message "FAILED" appears on the CRT.

If test routine #A runs successfully, a binary count sequence goes to data lines DI01 – DI08, allowing bus driver U23 to be partially verified with an oscilloscope. If these checks fail to locate a failure in the HP-IB circuitry, suspect U14 or U23.

A. Clock Check

With oscilloscope, verify four clock signals shown on Figure 8-35.

U61 pin 14
U60 pin 13
U60 pin 12
U48 pin 13

Dot Clk (4 MHz)
Clk (ϕ0) (2 MHz)
WR CLK (2 MHz)
ADC CLK (1 MHz)

B. CPU Address Check

Signature Analyzer connections:
CLOCK ⌥ A7TP8 (CLK ϕ0)
START ⌥ A7TP6 (A15)
STOP ⌥ A7TP6 (A15)
GND A7TP9
Remove jumper A7E1.

Switch A7S1A2 off. This causes the CPU (U50) to repeatedly execute instruction AND #$29. This generates a binary count sequence on the address bus that cycles through the contents of Program ROM U34. Since A7S1A2 disables the data multiplexer U20–U22, only program memory data should appear on the CPU data bus, d0–d7. All decoding logic tied to the address bus is also exercised for verification.

C. Address Multiplex Check

Signature Analyzer connections:
CLOCK ⌥ A7TP8 (CLK ϕ0)
START ⌥ A7TP6 (A15)
STOP ⌟ A7TP6 (A15)
GND A7TP9
Remove jumper A7E1.
Switch A7S1A4 and A7S1A5 on.

To verify operation of address multiplexers U37–U42, the binary count sequence on address bus A0 through A9 is checked at the inputs of System Memory, U6 and U7, and Stroke Memory, U8–U11.

Refer to Figure 8-1 for general signature analysis instructions.

Unless otherwise indicated, signature analysis is independent of plug-in control settings and can be performed with plug-in removed.

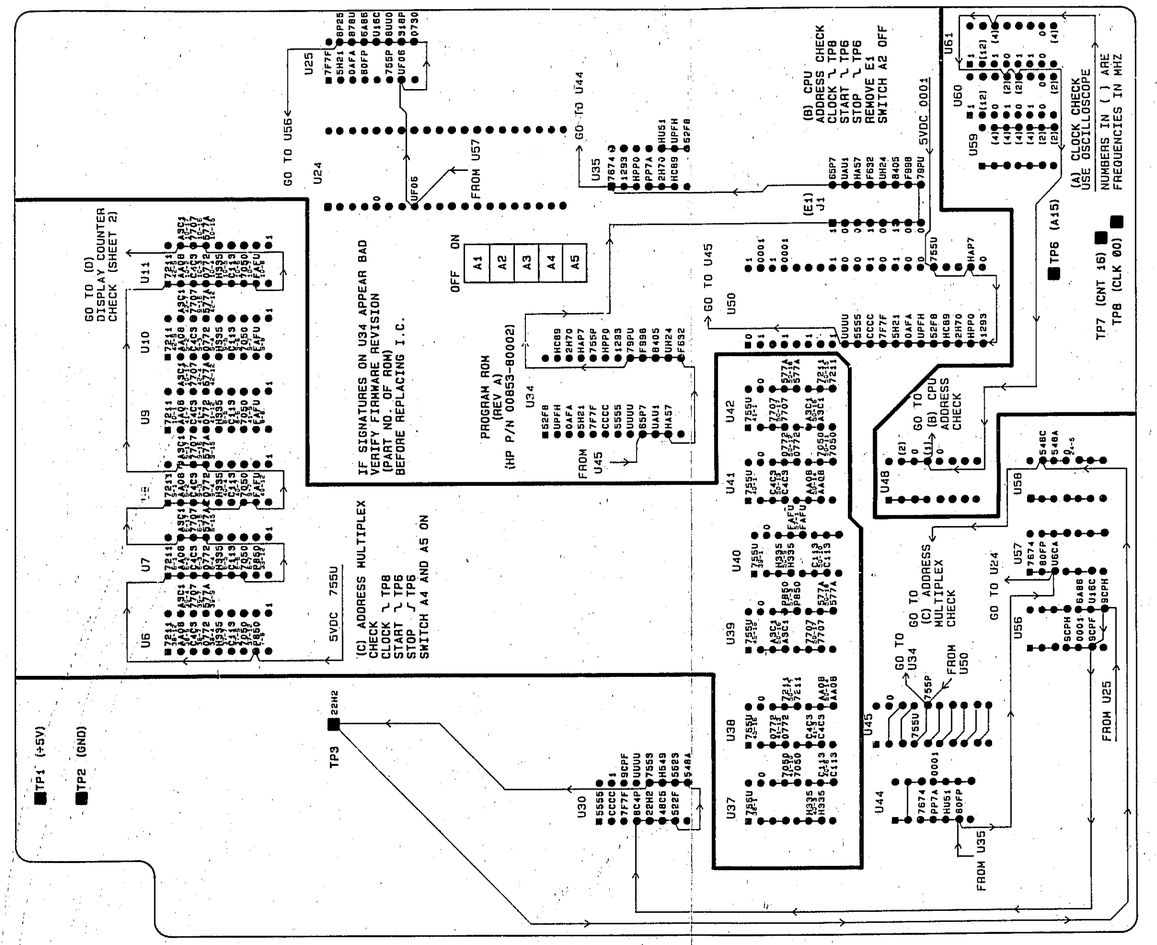


Figure 8-41. Processor Assembly A7, Signature Analysis Troubleshooting Diagram (1 of 4)

D. Display Counter Check

Signature Analyzer connections:
CLOCK ⌝⌞ A7TP8 (CLK Ø0)
START ⌝⌞ A7TP7 (CNT 16)
STOP ⌝⌞ A7TP7 (CNT 16)
GND A7TP9
Remove jumper A7E1.
Switch A7S1A5 ON.
Ground A7TP3 to A7TP2 with a short jumper.
Set spectrum analyzer and SWEEP TIME/DIV control to AUTO and SWEEP TRIGGER control to SINGLE (or remove plug-in from display mainframe).

Grounding A7TP3 forces a low at the enable inputs of counter U36. This causes counters U36, U27, and U48A to continuously cycle through the display count sequence, which appears on the counter bus, lines CNT2 – CNT16. All display logic circuits tied to the counter bus are exercised.

Note that START and STOP signals rely on proper operation of the three counters. If the gate light on the signature analyzer is not flashing, check the counter outputs in sequence to determine which counter stage has stopped.

E. Display Counter Multiplexer Check

Signature Analyzer connections:
CLOCK ⌝⌞ A7TP8 (CLK Ø0)
START ⌟⌜ A7TP6 (A15)
STOP ⌝⌞ A7TP6 (A15)
GND A7TP9
Remove jumper A7E1.
Switch A7S1A3 OFF. Switch A7S1A4 and A7S1A5 ON.
Remove ground jumper from A7TP3.

The display count sequence on the counter bus lines, CNT5 – CNT13, is checked at the outputs of System Memory and Stroke Memory address multiplexers, U37 – U42. Full operation of the address multiplexers is verified by this check if the Address Multiplex Check (C) has been performed.

Refer to Figure 8-1 for general signature analysis instructions.

Unless otherwise indicated, signature analysis is independent of plug-in control settings and can be performed with plug-in removed.

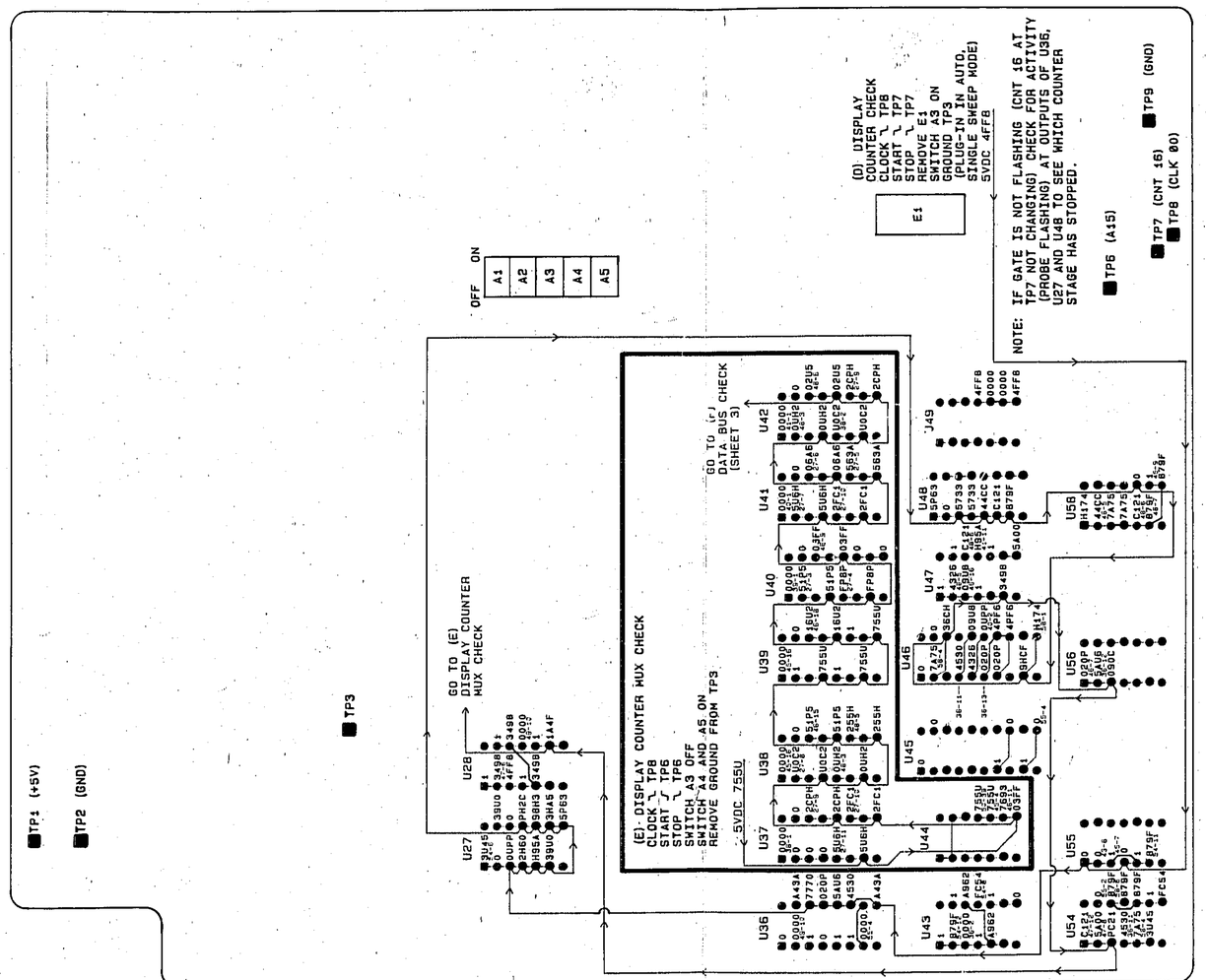


Figure 8-41. Processor Assembly A7, Signature Analysis Troubleshooting Diagram (2 of 4)

F. Data Bus Check

Signature Analyzer connections:
CLOCK ⌥ A7TP8 (CLK ϕ0)
START ⌥ A7TP3 (ANLG FST SWP EN)
STOP ⌥ A7TP3 (ANLG FST SWP EN)
GND A7TP9

Data Bus Test Routine Start-Up Procedure:
Install jumper A7E1.
Switch A7S1A3 on.
Switch A7S2A2, A7S1A4, and A7S1A5 off.
Set LINE switch OFF, and then ON, or ground A7TP5 (RESET) momentarily.
Then switch A7S1A2 on.
Set plug-in SWEEP TIME/DIV to MANUAL, or jumper A9TP1 (Interface Assembly A9) to ground at A7TP2.

When CPU U50 receives a power-up RESET signal with A7S1A2 off, a data bus test routine (stored in Program ROM U34) is activated. The CPU sends binary count sequences to data bus D0 – D15, CPU data bus d0 – d7, and data multiplexers U20 – U22. Locate data bus problems by checking data bus pins on System Memory RAMs U6 and U7 and Stroke Memory RAMs U8 – U11. This check also verifies memory write-enables lines from U26.

The +5 Vdc signature is correct only if the CPU (U50) is able to execute the test routine; suspect the CPU if it is incorrect. Signatures 6A0C or 0000 on U6 – U11 indicate a "hung" data bus line; use a logic pulser and current tracer to find the fault.

G. Stroke Blank Check

Signature Analyzer connections*:
CLOCK ⌥ A7U26 PIN 6 (LR/W)
START ⌥ A7TP3 (ANLG FST SWP EN)
STOP ⌥ A7TP3 (ANLG FST SWP EN)
GND A7TP9
Perform Data Bus Test Routine Start-Up Procedure (F).

The binary count sequence generated by the data bus test routine verifies the stroke blank signal (decoded on U57).

*For the next check move clock connection to A7U26, pin 6 (without turning power off).

H. Character Generator and Blanking Check

Signature Analyzer connections*:
CLOCK ⌥ A7U31 PIN 2 (DOT CLK)
START ⌥ A7TP3 (ANLG FST SWP EN)
STOP ⌥ A7TP3 (ANLG FST SWP EN)
GND A7TP9
Switch A7S1A1 off.
Perform Data Bus Test Routine Start-Up Procedure (F).

The binary count sequence generated by the data bus test routine verifies blanking logic (U1, U15 – U18, and U45) and character generator (U19, U28, and U31 – U33). Character columns are read from the character ROM U33 into shift registers U31 and U32, and shifted into the blanking logic (U17, U18, and U45).

Signatures on U19, U33, and parts of U31 and U32 require moving the CLOCK connection to A7TP8 (CLK ϕ0).

*For the next check move clock connection to A7U31, pin 2. Switch A7S1A1 off, without turning power off.

Refer to Figure 8-1 for general signature analysis instructions.

Unless otherwise indicated, signature analysis is independent of plug-in control settings and can be performed with plug-in removed.

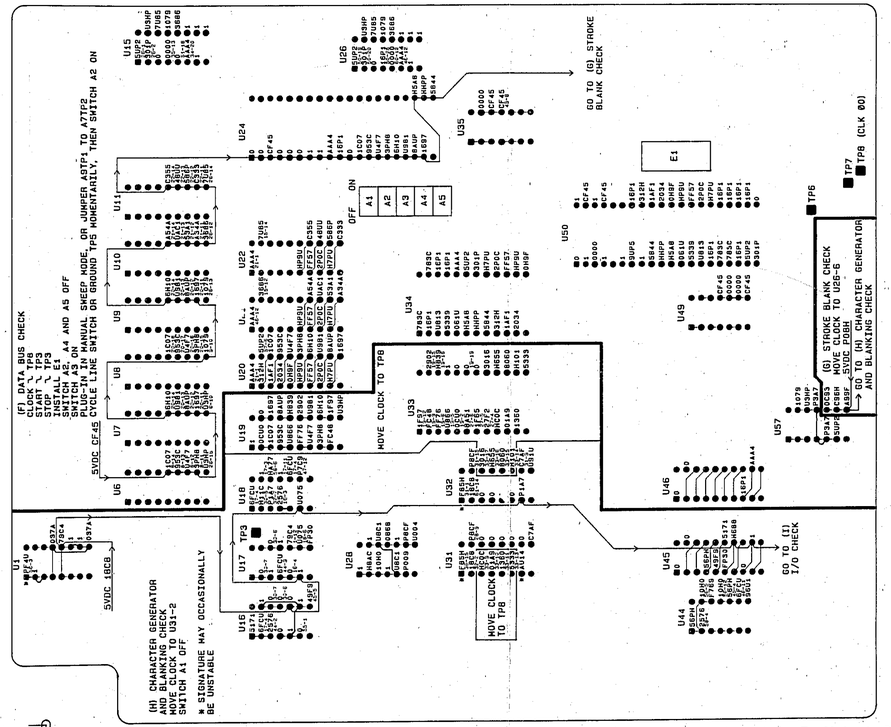


Figure 8-41. Processor Assembly A7, Signature Analysis Troubleshooting Diagram (3 of 4)

I. I/O Check

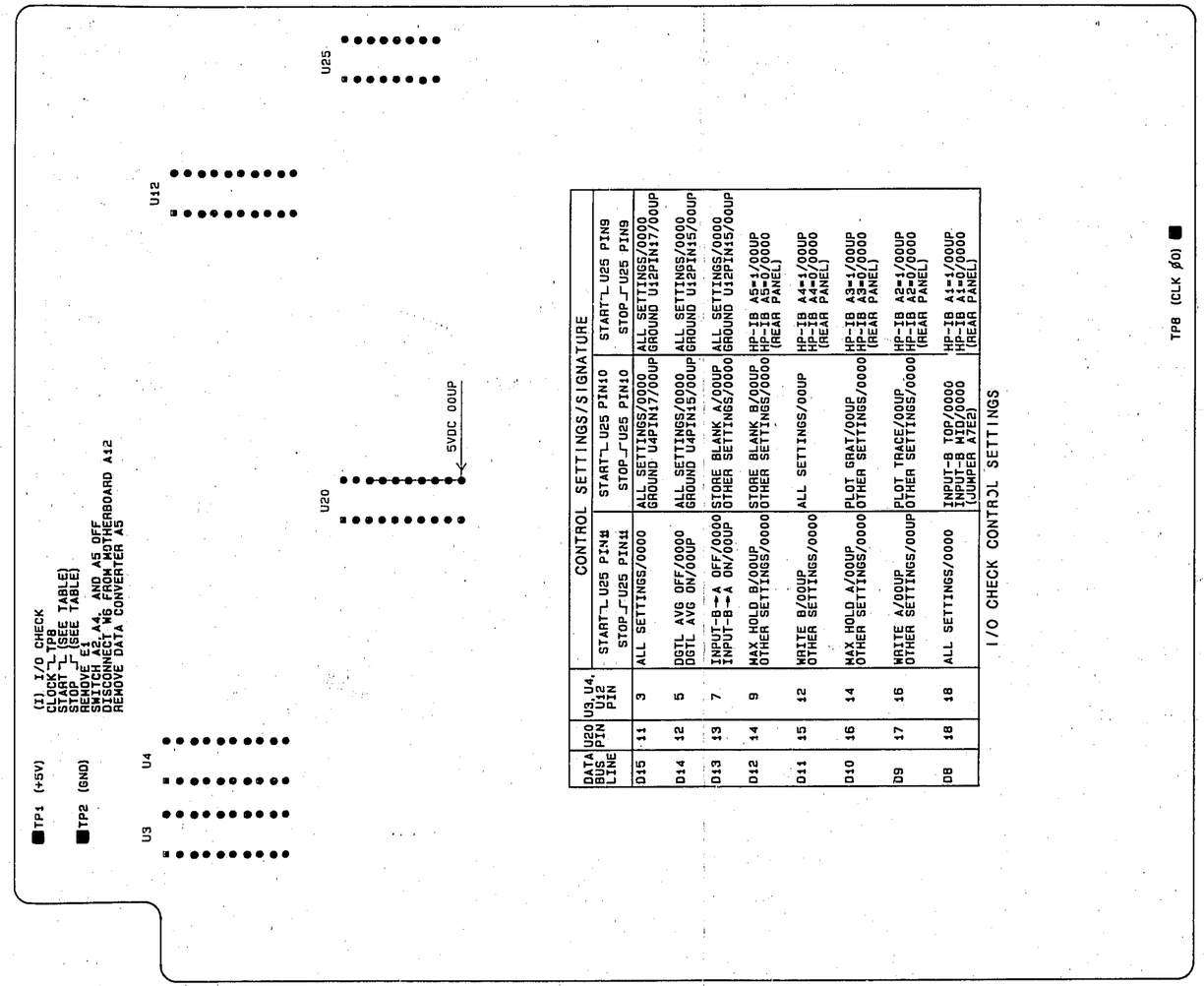
Signature Analyzer connections:
- CLOCK ⌝⌞ A7TP8 (CLK ø0)
- START ⌝⌞ (see table)
- STOP ⌞⌜ (see table)
- GND A7TP9

Remove Data Converter Assembly A5 from display mainframe.
Remove jumper A7E1.
Switch A7S1A2, A7S1A4, and A7S1A5 OFF.
Disconnect 14-wire ribbon cable W6 from Motherboard Assembly A12.
5 Vdc Signature = 00UP

The binary count sequence on address bus A0 – A15 enables I/O buffers U3, U4, and U12, driving the high-order data bus lines D8 – D15. Each I/O line is verified by changing control settings according to the table.

Refer to Figure 8-1 for general signature analysis instructions.

Unless otherwise indicated, signature analysis is independent of plug-in control settings and can be performed with plug-in removed.



CONTROL SETTINGS/SIGNATURE

DATA BUS LINE	U20 PIN	U3, U4, U12 PIN	START⌝⌞ U25 PIN11 / STOP⌞⌜U25 PIN11	START⌝⌞ U25 PIN10 / STOP⌞⌜U25 PIN10	START⌝⌞ U25 PIN9 / STOP⌞⌜U25 PIN9
D15	11	3	ALL SETTINGS/0000	ALL SETTINGS/0000 GROUND U4PIN17/00UP	ALL SETTINGS/0000 GROUND U12PIN17/00UP
D14	12	5	DGTL AVG OFF/0000 DGTL AVG ON/00UP	ALL SETTINGS/0000 GROUND U4PIN15/00UP	ALL SETTINGS/0000 GROUND U12PIN15/00UP
D13	13	7	INPUT-B→A OFF/0000 INPUT-B→A ON/00UP	STORE BLANK A/00UP OTHER SETTINGS/0000	ALL SETTINGS/0000 GROUND U12PIN15/00UP
D12	14	9	MAX HOLD B/00UP OTHER SETTINGS/0000	STORE BLANK B/00UP OTHER SETTINGS/0000	HP-IB A5=1/00UP HP-IB A5=0/0000 (REAR PANEL)
D11	15	12	WRITE B/00UP OTHER SETTINGS/0000	ALL SETTINGS/00UP	HP-IB A4=1/00UP HP-IB A4=0/0000 (REAR PANEL)
D10	16	14	MAX HOLD A/00UP OTHER SETTINGS/0000	PLOT GRAT/00UP OTHER SETTINGS/0000	HP-IB A3=1/00UP HP-IB A3=0/0000 (REAR PANEL)
D9	17	16	WRITE A/00UP OTHER SETTINGS/00UP	PLOT TRACE/00UP OTHER SETTINGS/0000	HP-IB A2=1/00UP HP-IB A2=0/0000 (REAR PANEL)
D8	18	18	ALL SETTINGS/0000	INPUT-B TOP/0000 INPUT-B MID/0000 (JUMPER A7E2)	HP-IB A1=1/00UP HP-IB A1=0/0000 (REAR PANEL)

I/O CHECK CONTROL SETTINGS

Figure 8-41. Processor Assembly A7, Signature Analysis Troubleshooting Diagram (4 of 4)

A7
PROCESSOR ASSEMBLY
00853-60008

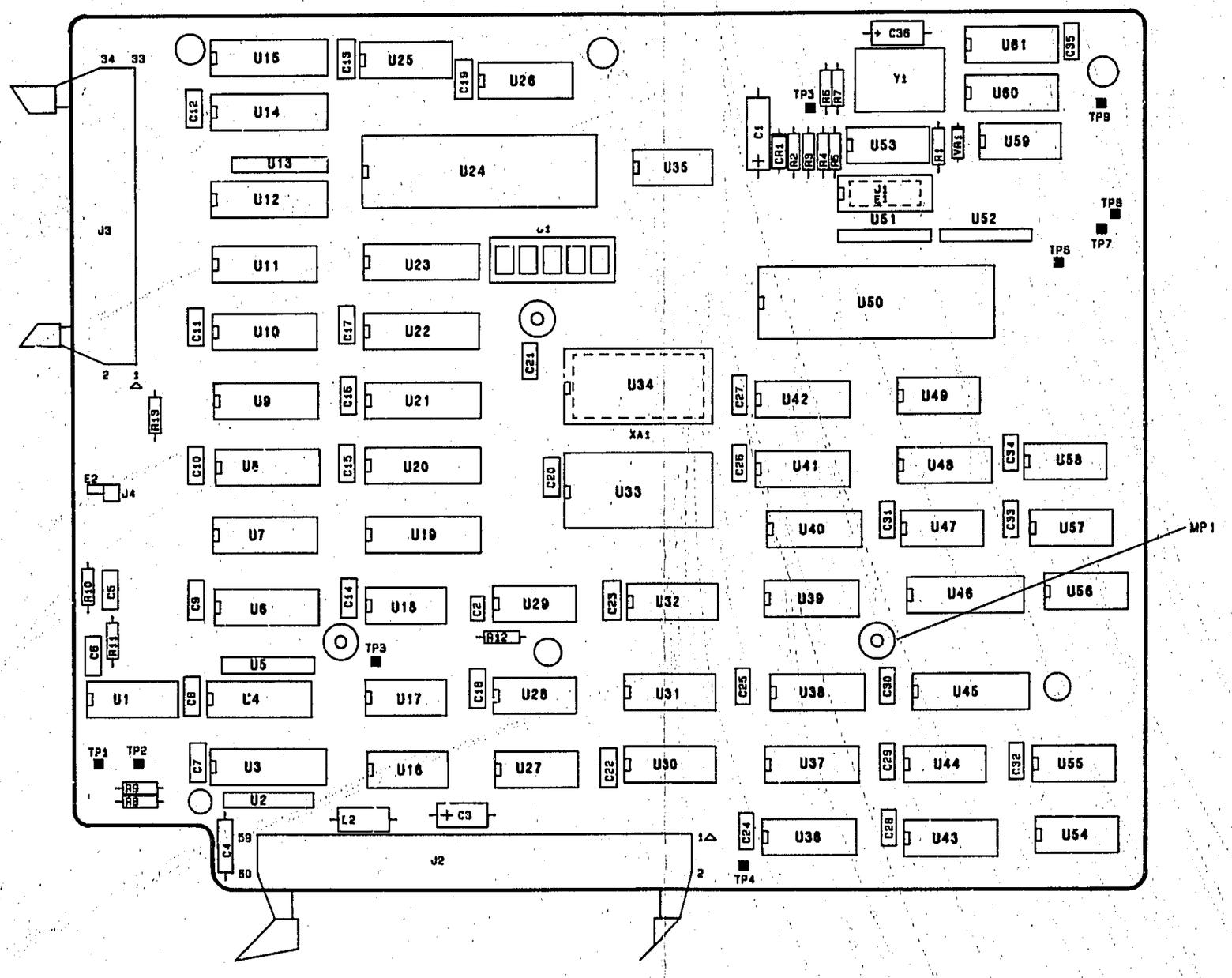
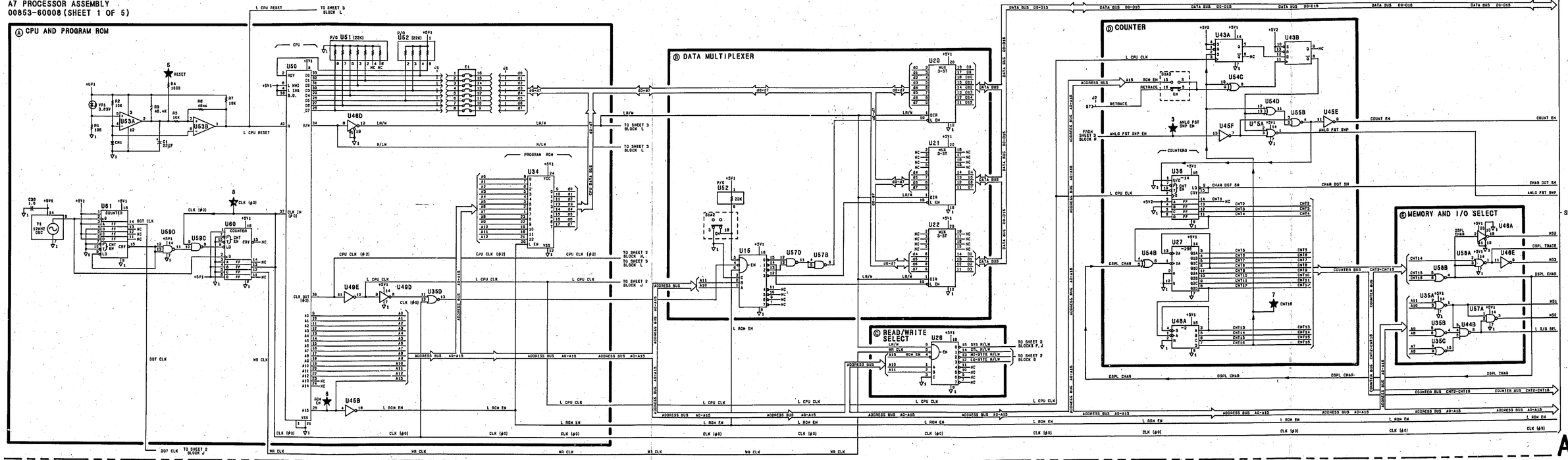


FIGURE 8-42. PROCESSOR ASSEMBLY A7, COMPONENT LOCATIONS

A7 PROCESSOR ASSEMBLY
00853-60008 (SHEET 1 OF 5)



A7

SERIAL PREFIX: 2223A

FIGURE 8-43. PROCESSOR ASSEMBLY A7, SCHEMATIC DIAGRAM (1 OF 5)

8-81/8-82

A7 PROCESSOR ASSEMBLY 00853-60008 (SHEET 2 OF 5)

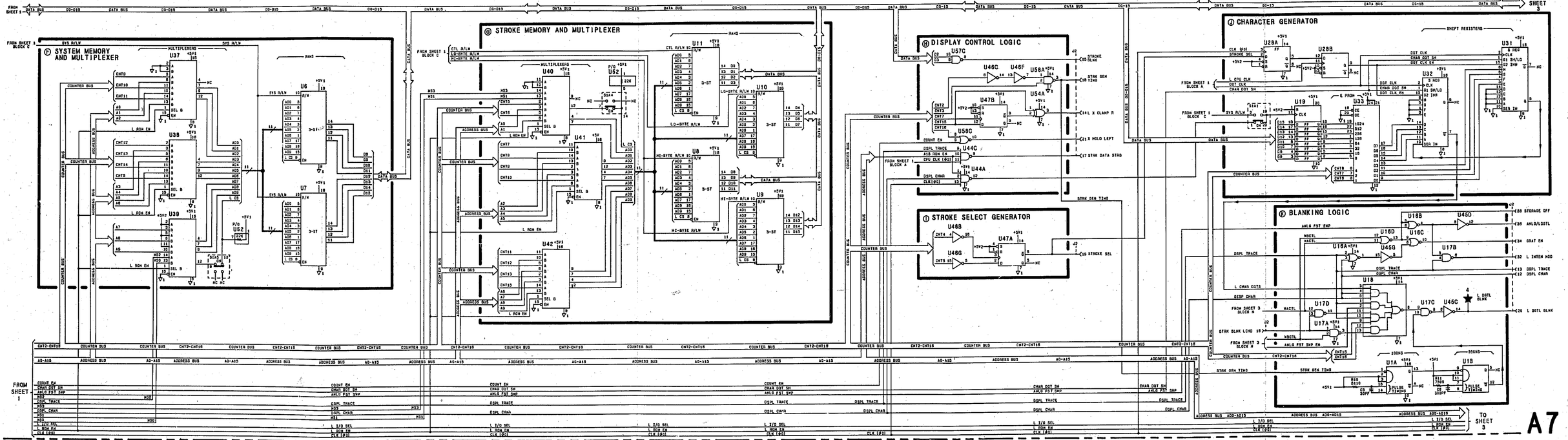
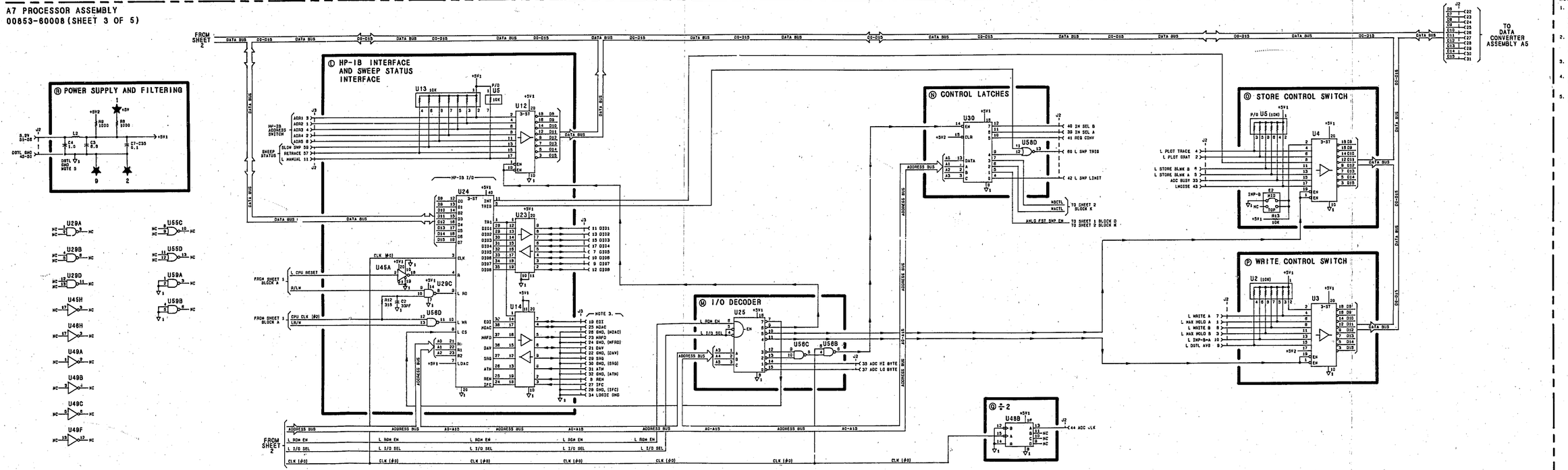


FIGURE 8-43. PROCESSOR ASSEMBLY A7, SCHEMATIC DIAGRAM (2 OF 5)

8-83/8-84

A7 PROCESSOR ASSEMBLY
00853-60008 (SHEET 3 OF 5)



NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. FOR COMPLETE REFERENCE DESIGNATION, PREFIX ABBREVIATION WITH ASSEMBLY DESIGNATION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IS IN OHMS (Ω) CAPACITANCE IS IN MICROFARADS (μF) INDUCTANCE IS IN MICROHENRIES (μH)
3. HP-IB SIGNAL WIRE AND ITS ASSOCIATED GROUND WIRE ARE A TWISTED PAIR.
4. UNLESS OTHERWISE INDICATED, SIGNALS ENTER AT LEFT SIDE AND EXIT AT RIGHT SIDE OF FUNCTION BLOCKS.
5. DGTL GND CONNECTS TO CHASSIS (GND) ON MOTHERBOARD.

A7

FIGURE 8-43. PROCESSOR ASSEMBLY A7, SCHEMATIC DIAGRAM (3 OF 5)

A7 PROCESSOR ASSEMBLY
00853-60008 (SHEET 4 OF 5)

J3

PIN	SIGNAL	TO FROM	FUNCTION BLOCK
1	ADR2	A10P1-1	L
2	ADR4	A10P1-2	L
3	ADR1	A10P1-3	L
4	ADR3	A10P1-4	L
5	NC		
6	ADR5	A10P1-6	L
7	D105	A10P1-7	L
8	REN	A10P1-8	L
9	D107	A10P1-9	L
10	D106	A10P1-6	L
11	D101	A10P1-11	L
12	D100	A10P1-12	L
13	D102	A10P1-13	L
14	NC		
15	D103	A10P1-15	L
16	NC		
17	D104	A10P1-17	L
18	NC		
19	EOI	A10P1-19	L
20	NC		
21	DAV	A10P1-21	L
22	GND, (DAV)	A10P1-22	L
23	NRFD	A10P1-23	L
24	GND, (NRFD)	A10P1-24	L
25	NDAC	A10P1-25	L
26	GND, (NDAC)	A10P1-26	L
27	IFC	A10P1-27	L
28	GND, (IFC)	A10P1-28	L
29	SRQ	A10P1-29	L
30	GND, (SRQ)	A10P1-30	L
31	ATN	A10P1-31	L
32	GND, (ATN)	A10P1-32	L
33	NC		
34	LOGIC GND	A10P1-34	L

J2

PIN	SIGNAL	TO FROM	FUNCTION BLOCK
1	L MAX HOLD A	A1A1P1-12	P
2	L PLOT GRAT	A1A1P1-16	O
3	L MAX HOLD B	A1A1P1-14	P
4	L PLOT TRACE	A1A1P1-18	O
5	L STORE BLNK A	A1A1P1-20	O
6	L STORE BLNK B	A1A1P1-19	O
7	L WRITE A	A1A1P1-17	P
8	L WRITE B	A1A1P1-15	P
9	L DGTL AVG	A1A1P1-10	P
10	L INP-B-A	A1A1P1-13	P
11	LMANUAL	A9J1-6	L
12	DSPL CHAR	A5P1-30	K
13	DSPL TRACE	A5P1-31	K
14	L X CLAMP B	A5P1-6	H
15	STROKE BLNK	A5P1-32	H
16	STRK BLNK LCHD	A5P1-7	K
17	STRK DATA STRB	A5P1-33	H
18	STRK GEN TIMG	A5P1-8	H
19	STROKE SEL	A5P1-34	I
20	L DGTL BLNK	A5P1-7	K
21	X HOLD LEFT	A5P1-9	H
22	D6	A5P1-35	
23	D7	A5P1-10	
24	D8	A5P1-36	
25	D9	A5P1-11	
26	D10	A5P1-37	
27	D11	A5P1-12	
28	D12	A5P1-38	
29	D13	A5P1-13	
30	D14	A5P1-39	
31	D15	A5P1-14	
32	L INTEN MOD	A5P1-37	K
33	A/D BUSY	A5P1-40	O
34	GRAT EN	A5P1-36	K
35	ADC HI BYTE	A5P1-15	M
36	ANLG/LOGTL	A5P1-4	K
37	ADC LO BYTE	A5P1-41	M
38	NC		
39	IN SEL A	A5P1-16	N
40	IN SEL B	A5P1-42	N
41	REQ CONV	A5P1-17	N
42	L SWP LIMIT	A9J1-5	N
43	LNOISE	A5P1-19	O
44	ADC CLK	A7P1-18	Q
45	DGTL GND	NOTE 5	R
46	DGTL GND	NOTE 5	R
47	DGTL GND	NOTE 5	R
48	DGTL GND	NOTE 5	R
49	DGTL GND	NOTE 5	R
50	DGTL GND	NOTE 5	R
51	+5V	A1A1P1-7	R
52	+5V	A1A1P1-7	R
53	+5V	A1A1P1-7	R
54	+5V	A1A1P1-7	R
55	+5V	A1A1P1-7	R
56	+5V	A1A1P1-7	R
57	RETRACE	A9PJ1-10	L
58	STORAGE OFF	A9PJ1-8	K
59	SLOW SWP	A9PJ1-7	L
60	L SWP TRIG	A9PJ1-9	N

A7

SERIAL PREFIX: 2223A

Figure 8-43. Processor Assembly A7, Schematic Diagram (4 of 5)

MNEMONICS	DESCRIPTION
ADC BUSY	ANALOG TO DIGITAL CONVERSION BUSY
ADC CLK	ADC CLOCK
ADC HI BYTE	ADC HIGH-BYTE
ADC LO BYTE	ADC LOW-BYTE
ANLG/LDGTL	ANALOG/LOW-DIGITAL
ANLG FST SWP	ANALOG FAST SWEEP
ANLG FST SWP EN	ANALOG FAST SWEEP ENABLE
ATN	ATTENTION
CHAR DOT	CHARACTER DOT
CHAR DOT SH	CHARACTER DOT SHIFT
CLK ϕO	CLOCK ϕO
COUNT EN	COUNT ENABLE
CPU CLK	CENTRAL PROCESSING UNIT CLOCK
CTL R/LW	CONTROL READ/LOW-WRITE
DAV	DATA VALID
DGTL GND	DIGITAL GROUND
DOT CLK EN	DOT CLOCK ENABLE
DSPL CHAR	DISPLAY CHARACTER
DSPL TRACE	DISPLAY TRACE
EOI	END OR IDENTIFY
GRAT EN	GRATICULE ENABLE
HI-BYTE R/LW	HIGH-BYTE READ/LOW-WRITE
IFC	INTERFACE CLEAR
IN SEL A	INPUT SELECT A
IN SEL B	INPUT SELECT B
L CHAR DOTS	LOW CHARACTER DOTS
L CPU CLK	LOW CENTRAL PROCESSING UNIT CLOCK
L CPU RESET	LOW CPU RESET
L DGTL AVG	LOW DIGITAL AVERAGE
L DGTL BLNK	LOW DIGITAL BLANK
INP-B=A	LOW INPUT MINUS B EQUALS A
L INTEN MOD	LOW INTENSITY MODULATION
L I/O SEL	LOW INPUT/OUTPUT SELECT
L MAX HOLD A	LOW MAXIMUM HOLD A
L MAX HOLD B	LOW MAXIMUM HOLD B
L PLOT GRAT	LOW PLOT GRATICULE
L PLOT TRACE	LOW PLOT TRACE
L ROM EN	LOW READ-ONLY MEMORY ENABLE
L STORE BLNK A	LOW STORE BLANK A
L STORE BLNK B	LOW STORE BLANK B
L SWP TRIG	LOW SWEEP TRIGGER
L SWP LIMIT	LOW SWEEP LIMIT
L WRITE A	LOW WRITE A
L WRITE B	LOW WRITE B
L X CLAMP R	LOW X CLAMP RIGHT
LMANUAL	LOW MANUAL
LNOISE	LOW NOISE
LO-BYTE R/LW	LOW-BYTE READ/LOW-WRITE
LR/W	LOW-READ/WRITE
MS0	MEMORY SELECT 0
MS1	MEMORY SELECT 1
MS2	MEMORY SELECT 2
MS3	MEMORY SELECT 3
NDAC	NOT DATA ACCEPTED
NRFD	NOT READY FOR DATA
REN	REMOTE ENABLE
REQ CONV	REQUEST CONVERSION
R/LW	READ/LOW-WRITE
ROM EN	READ-ONLY-MEMORY ENABLE
SLOW SWP	SLOW SWEEP
SRQ	SERVICE REQUEST
STRK BLNK LCHD	STROKE BLANK LATCHED
STRK DATA STRB	STROKE DATA STROBE
STRK GEN TIMG	STROKE GENERATOR TIMING
STROKE SEL	STROKE SELECT
SYS R/LW	SYSTEM READ/LOW-WRITE
WR CLK	WRITE CLOCK
X HOLD '	X HOLD LEFT

A7

SERIAL PREFIX: 2223A

Figure 8-43. Processor Assembly A7, Schematic Diagram (5 of 5)

INTERFACE ASSEMBLY A9, CIRCUIT DESCRIPTION

Interface Assembly A9 processes the analog vertical, sweep, and penlift signals from the plug-in to drive circuitry in the XYZ Amplifier Assembly A6 and Data Converter Assembly A5. Also, the input sweep rate is detected and used to control the display mode.

This assembly generates an error signal which is fed back to the plug-in. This error signal limits the AUTO TIME/DIV sweep rate when digital display mode is selected. A comparator signals Processor Assembly A7 when manual sweep mode is active. The Interface Assembly buffers a sweep trigger signal generated by the Processor Assembly. It also senses the plug-in sweep speed and initiates mixed mode. (For detailed description of mixed mode, refer to Counter circuit description of Processor Assembly A7.)

Video Amplifier Ⓐ

The differential vertical output from the plug-in is attenuated in the Interface Assembly, forming the VIDEO input for the XYZ amplifiers and the analog-to-digital converters in assemblies A5 and A6.

Transistor Q8 amplifies the difference of the signals at its bases and drives emitter follower Q7. The Q7 output is fed back through R7 to the inverting base of Q8, where it is summed with one of the differential inputs fed through R2. The other differential input is divided by R1 and R3 and applied to the noninverting base of Q8. The voltage gain equals R7/R2 or R3/R1. Resistor R8 provides output voltage offset. When the two inputs are equal, TP4 is about 0.4V.

Resistor R5 sets the emitter current in Q8. VR1 determines Q7 emitter voltage. Resistor R4 sets the collector current in the inverting half of Q8. Bias current for Q7 is provided by R10. Supply filtering is provided by R6, C1, C2, C7, and L1. The amplifier is isolated from external loads to prevent oscillations by R9 and R11.

Sweep Buffer Ⓑ

When switch S1 is set to the INT position, the −5V and +5V sweep signal from the plug-in passes through unity-gain amplifier U5 to the XYZ Amplifier Assembly and the Data Converter Assembly. The sweep signal also passes through R31 to the rear-panel HORIZ (SWEEP) output. Resistor R32, CR5 and CR6 prevent the U5 input from exceeding power supply limits.

When switch S1 is set to the EXT position, the signal present at the rear-panel HORIZ (SWEEP) becomes the sweep input to U5. When no sweep signal is present, R30 holds the U5 input at 0V.

Automatic Sweep Time (AST) Limiter, General Description

Figure 8-44 illustrates how the basic sweep circuitry in the plug-in and the AST limiter circuitry interact. In the plug-in, a current source feeds an integrating capacitor, forming a ramp. When the ramp voltage has increased to +5V, a comparator triggers a switch to reset the integrating capacitor to −5V and the cycle repeats. The value of the current source is proportional to the slope of the sweep voltage waveform. When AUTO TIME/DIV is selected, the current source is varied by both the plug-in and Interface Assembly A9. The plug-in varies the current source with resistors (R), according to plug-in, front-panel control settings. The Interface Assembly varies the current source with feedback current IFB.

The sweep rate is detected by differentiating the sweep waveform; the output of U4A is negative when the slope of the sweep exceeds a threshold value determined by R13. This causes the output of integrator U4B to increase, producing more feedback current for the plug-in. This decreases the current feeding the integrating capacitor, decreasing the slope of the sweep ramp.

Sweep Differentiator Ⓒ

Summing amplifier U4A produces an output proportional to the slope of the sweep voltage waveform. The sweep voltage is applied across C3, producing a current proportional to the sweep voltage change per unit time.

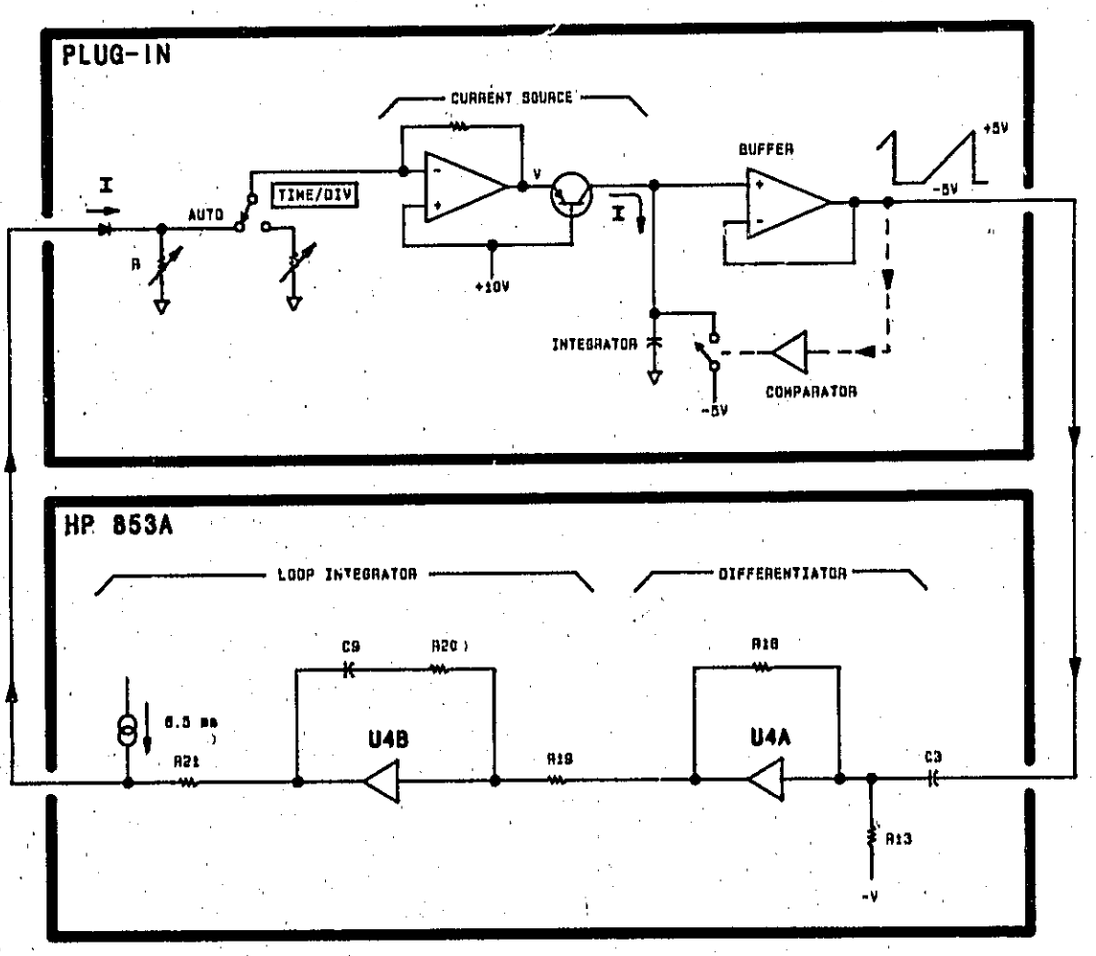


Figure 8-44. Automatic Sweep Time Limiter

The constant current in R13 is subtracted from the current produced by C3. The difference passes through R18. When the currents produced by R13 and C3 are equal, U4A output is zero. During a sweep, the U4A output is positive or negative when the C3 current is less or greater than the current through R13. During retrace, C3 current is negligible and R13 biases the U4A output positive.

When a digital display mode other than DGTL AVG is active, Q6 is off and R14 and R15 produce a 1.2V drop across R13. This corresponds to a 120 V/sec slope, equivalent to a 8.3 msec/DIV sweep. When DGTL AVG mode is active, Q6 is on and R14 – 16 produce a 0.66V drop across R13. This yields a 66 V/sec slope, equivalent to a 15 msec/DIV sweep.

AST Loop Integrator (D)

Amplifier U4B integrates the error-voltage output of U4A to provide a feedback signal to the plug-in. Resistor R19 determines the current integrated by C8. Resistor R20 provides feedback loop compensation. Diode CR2 prevents U4B output from being less than −0.6V.

The U4B output is converted by R21, CR4, and Q4 to current. The collector current of Q4 is the same as Q4B since R24 and R25 are equal. Q4A is a 6.5 mA current source. When the AST limit feedback loop is active during auto sweep times and digital display mode, Q4A collector voltage is about +11V. When U4B output is high, CR4 is reverse-biased and all current from Q4A goes to the plug-in, slowing its sweep. As U4B output decreases, CR4 conducts through R21, diverting Q4A current from the plug-in, allowing the sweep rate to increase.

Switch Q3 disables the AST limit feedback loop when both STORE BLANK buttons are pressed. Current flows through R27, turning on Q3. No current flows to the plug-in. When no input connection is made, R28 provides base current to Q3.

For troubleshooting, ground TP7. This turns Q3 off and enables the AST limit feedback loop.

Slow Sweep Detect E

When digital display mode and calibrated sweep times are active, the feedback loop is disabled and the output of integrator U4B ramps up or down according to the sweep rate. Comparator U1A provides an indication to the Processor Assembly of the sweep rate. For sweeps slower than the threshold determined by R13 (8.3 ms/DIV or 15 msec/DIV), U4A output is positive during the forward-portion of the sweep. This causes the output of integrator U4B to decrease to −0.6V. Thus, the inverting input of U1A is less than the noninverting input determined by R22 and R23; this forces U1A output high. For sweeps faster than the threshold (R13), U4B output increases. The inverting input of U1A is then higher than the noninverting input determined by R22 and R24; U1A output goes low.

Comparators F

Comparators U1B and U1C convert PENLIFT to a RETRACE signal for Processor Assembly A7, and a switching signal for Q5. PENLIFT is 0V during the sweep, and +15V during retrace. PENLIFT is compared with +5 Vdc (U2R5 and U3R5). When PENLIFT is greater than +15V, CR3 and U2R6 protect the comparator inputs.

The LMANUAL signal notifies Processor Assembly when manual mode is active. The output of U1D is normally at +5V; it is 0V during manual mode.

Sweep Trigger G

Transistors Q1 and Q2 convert L SWP TRIG to levels compatible with the the plug-in. Transistors Q1 and Q2 are normally off. To trigger a sweep, L SWP TRIG initially goes to 0V, then returns to +5V. Transistor Q1 turns on. Current through R36 turns Q2 on. The collector of Q2 goes to +15V and resets the sweep. When Q2 turns off, its output returns to −15V, triggering the sweep.

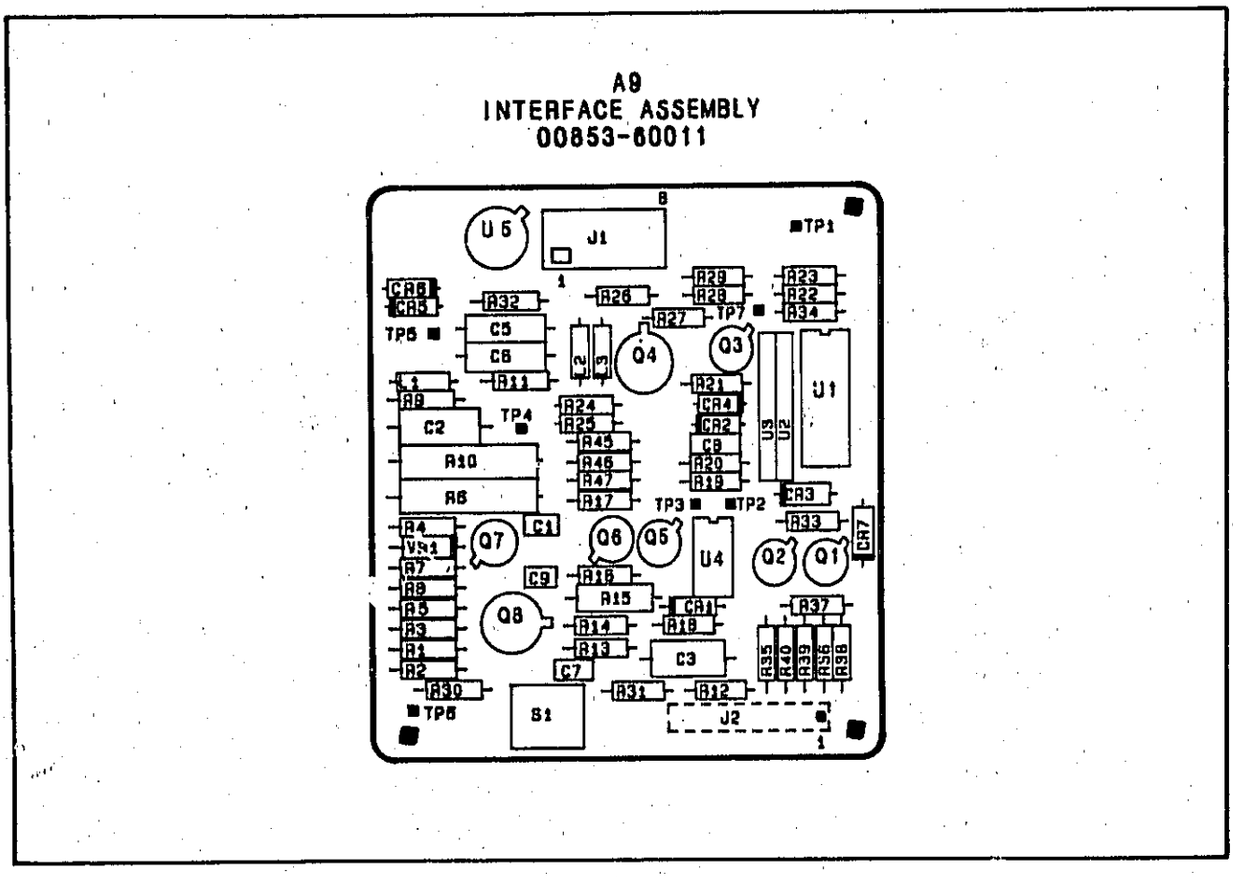
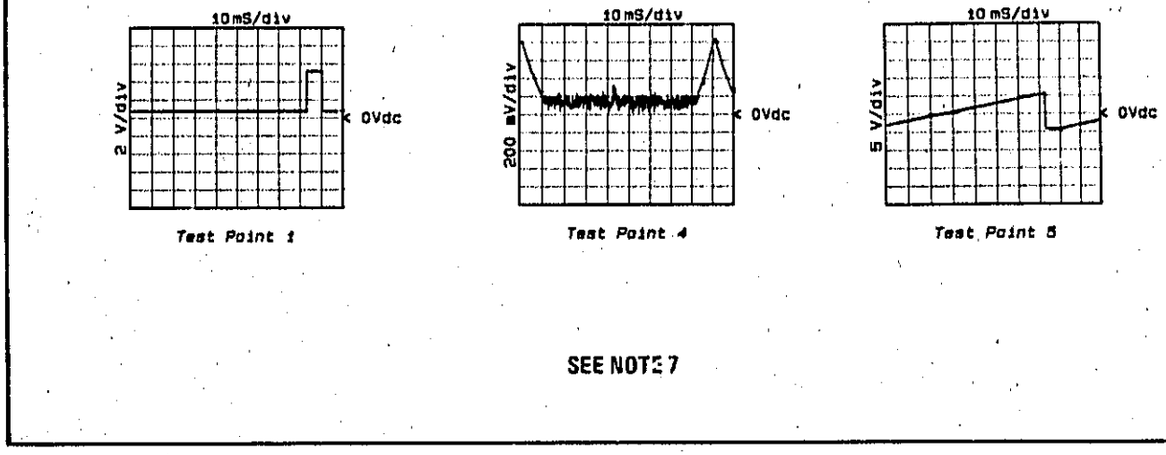


Figure 8-45. Interface Assembly A9, Component Locations



J1

PIN	SIGNAL	TO/FROM	FUNCTION BLOCK
1	NC		
2	+15V	A3J2-5	H
3	-15V	A3J2-7	H
4	AMLG BLNK	A9P3-32	
5	L SWP LIMIT	A7J2-42	C
6	LMANUAL	A7J2-31	F
7	SLOW SWP	A7J2-59	E
8	STORAGE OFF	A7J2-58	D
9	L SWP TRIG	A7J2-60	G
10	RETRACE	A7J2-57	F
11	GND	NOTE 4	
12	RETURN	NOTE 4	
13	VIDEO	A9P3-50 A9P1-50	A
14	SWEEP	A9P3-44 A9P1-42	B

PLUG-IN
REFER TO PLUG-IN MANUAL FOR COMPLETE CIRCUITRY

FROM PLUG-IN POWER SUPPLY ASSEMBLY A9

+12.8V
+15V
+150V
GND

30Y3-P
30Y3-S (LINE TRIGGER)
BEAM FINDER
-12.8V
+15V
+150V
L HORN
+10V ENABLE
TO PLUG-IN POWER SUPPLY ASSEMBLY A9

DETECTOR AND LOG AMPLIFIER
VERT POSN
VERT GAIN
BOTTOM DEFLECTION CONTACT
TOP DEFLECTION CONTACT
AUX VERT
IF OUT
SLOW SWEEP
APPROX +10V
AST
+5V
-5V
HORIZONTAL OUTPUT
REAR PANEL (VERTICAL DEFLEC)
REAR PANEL (HORIZ DEFLEC)
REAR PANEL (BLANK(REMOTE))
PENLIFT
+15V
0V
S17 NOTE 8
MMANUAL
BLANKING
-12.8V
P/O SWEEP TRIGGER
SINGLE
EXT TRIGGER
NOTE 8

A12 MOTHERBOARD

A9 INTERFACE ASSEMBLY 00853-60011

Ⓐ VIDEO AMPLIFIER
Ⓑ SWEEP BUFFER
Ⓒ SWEEP DIFFERENTIATOR
Ⓓ AST LOOP INTEGRATOR
Ⓔ SLOW SWEEP DETECT
Ⓕ COMPARATORS
Ⓖ SWEEP TRIGGER
Ⓗ SUPPLY FILTERING

SERIAL PREFIX: 2223A

A12 MOTHERBOARD

VIDEO
SLOW SWEEP
GND
STORAGE OFF
L SWP LIMIT
SWEEP
RETRACE
LMANUAL
AMLG BLNK
L SWP TRIG

NOTES:

1. REFERENCE DESIGNATORS WITHIN THIS ASSEMBLY ARE ABBREVIATED. FOR COMPLETE REFERENCE DESIGNATION, PREFIX ABBREVIATION WITH ASSEMBLY DESIGNATION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IS IN OHMS (Ω) CAPACITANCE IS IN MICROFARADS (μF) INDUCTANCE IS IN MICROHENRIES (μH)
3. UNLESS OTHERWISE INDICATED, SIGNALS ENTER AT LEFT SIDE AND EXIT AT RIGHT SIDE OF FUNCTION BLOCKS.
4. ALL GROUNDS CONNECT TO CHASSIS (GND) AT MOTHERBOARD.
5. TOP VIEW OF A6Q5, A9Q8
6. MNEMONIC TABLE:

MNEMONIC	DESCRIPTION
AMLG BLNK	ANALOG BLANK
AST	AUTOMATIC SWEEP TIME
AUX VERT	AUXILIARY VERTICAL
EXT TRIG	EXTERNAL TRIGGER
LMANUAL	LOW MANUAL
L SWP LIMIT	LOW SWEEP LIMIT
L SWP TRIG	LOW SWEEP TRIGGER
MMANUAL	HIGH MANUAL

7. REFER TO TABLE 8-3 FOR MEASUREMENT CONDITIONS.
8. THESE COMPONENTS ADDED TO MAKE THE HP853A, HP853B, AND HP853A PLUG-INS COMPATIBLE WITH THE HP853A.

A9

FIGURE 8-48. INTERFACE ASSEMBLY A9, SCHEMATIC DIAGRAM

A10

HP-IB INTERCONNECT ASSEMBLY

00853-60009

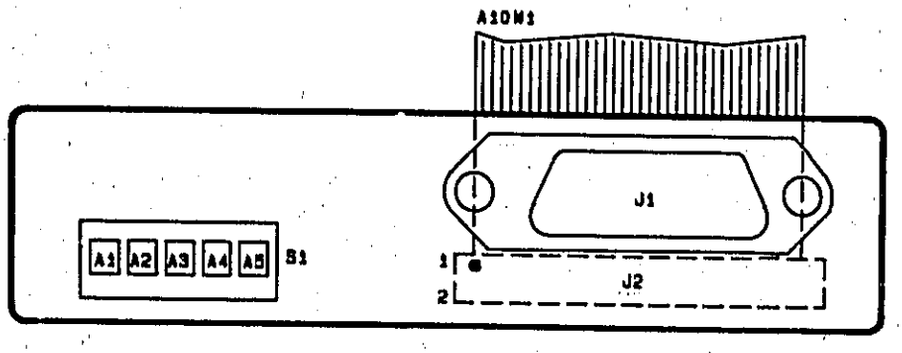
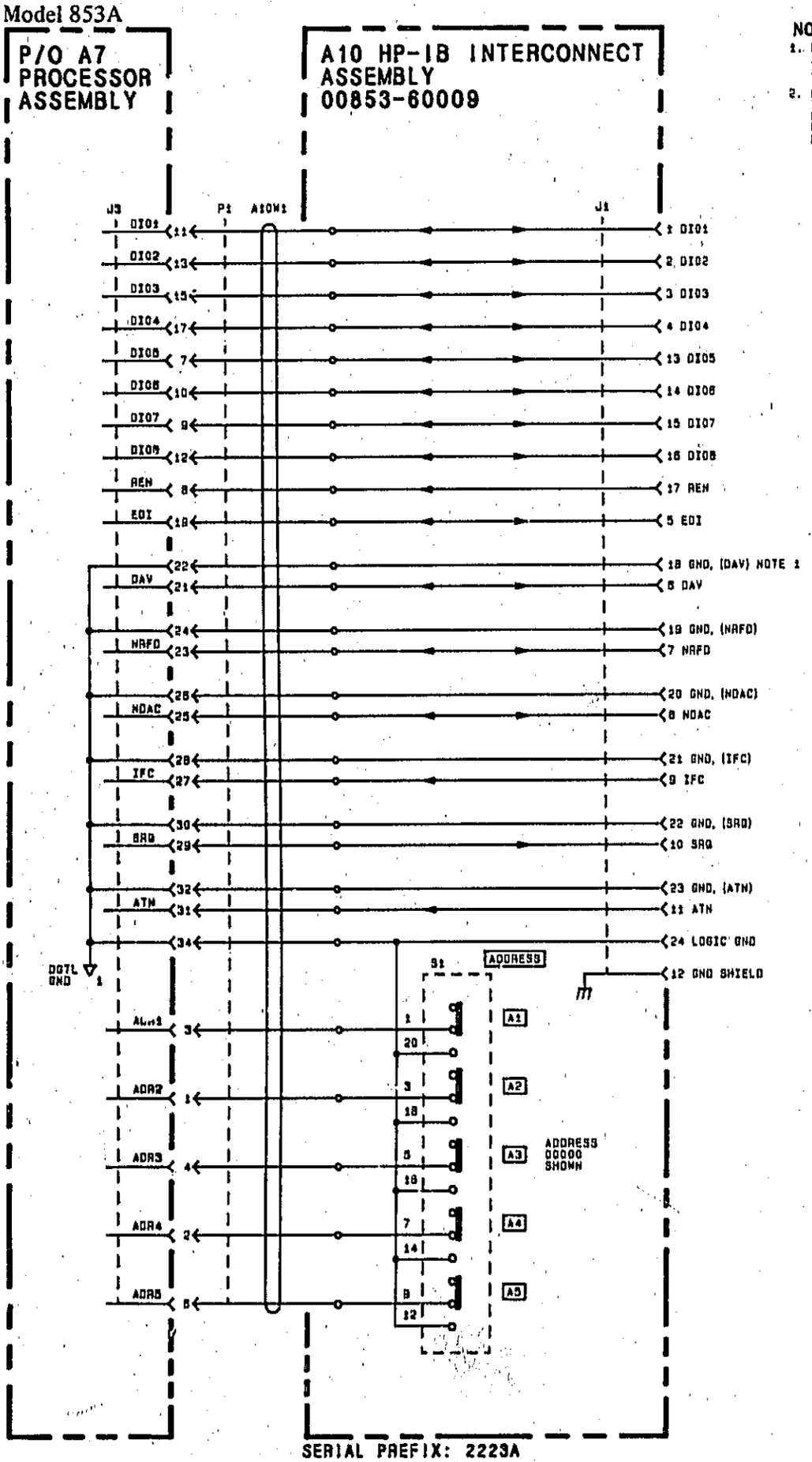


Figure 8-47. Interconnect Assembly A10, Component Locations



A10

Figure 8-48. HP-IB Interconnect Assembly A10, Schematic Diagram

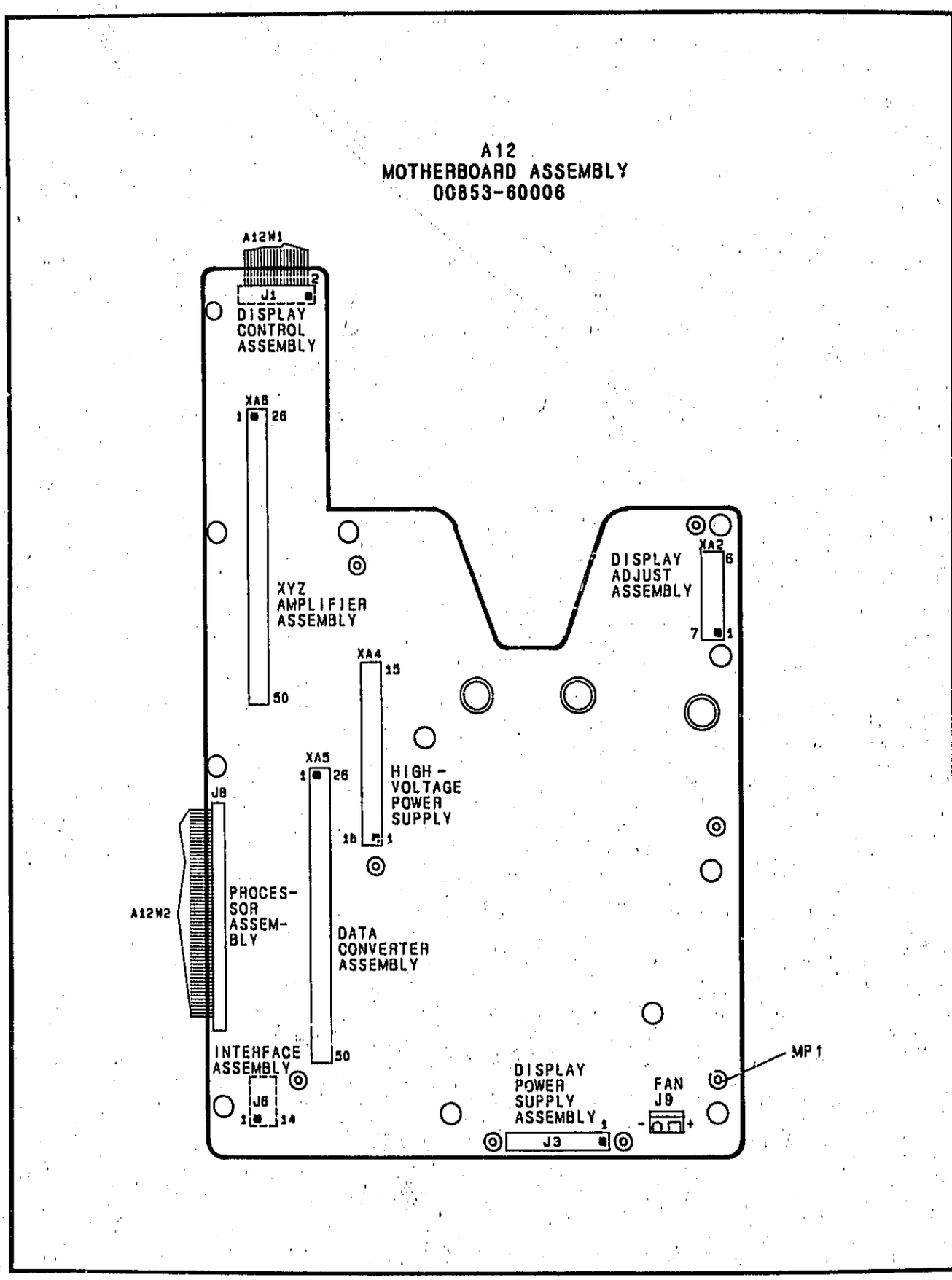


Figure 8-49. Motherboard Assembly A12, Component Locations

A12 MOTHERBOARD ASSEMBLY (00853-60006)

NOTES:

1. **Boldface indicates assembly where signal originates.**
2. **ANLG GND (▽), DGTL GND (▽$_1$), RETURN (▽$_2$), CTL GATE GND (▽$_3$), BUFFER GND (▽$_4$), and REG GND (▽$_6$) short to chassis at Motherboard Assembly A12. HC GND passes through Motherboard Assembly A12 and Display Power Supply Assembly A3. It connects to GND at Plug-in Power Supply Assembly A8. (See Figure 8-12.)**

	Display Control Assembly A1A1J1	Display Adjust Assembly A2P1	Display Power Supply Assembly A3J2	High-Voltage Power Supply Assembly A4P1	Data Converter Assembly A5P1	XYZ Amplifier Assembly A6P1	Processor Assembly A7J2	Interface Assembly A5J1	Fan Module Assembly (A13) A12J9
+158V	–	–	**1**	–	–	19,44	–	–	–
+158V SW	–	–	–	12,27	–	**20,45**	–	–	–
+15V	–	1,7	**6**	11,26	1,26	21,46	–	2	–
+26V UNREG	–	–	**4**	14,29	–	–	–	–	–
+5V	7	–	**12,13,14**	–	21,46	–	51,52,53 54,55,56	–	–
–15V	–	2,8	**7**	10,25	3,28	23,48	–	3	–
–FAN	–	–	**3**	–	–	–	–	–	2
ADC BUSY	–	–	–	–	**40**	–	33	–	–
ADC CLK	–	–	–	–	18	–	**44**	–	–
ADC HI BYTE	–	–	–	–	15	–	**35**	–	–
ADC LO BYTE	–	–	–	–	41	–	**37**	–	–
ANLG/LDGTL	–	–	–	–	–	4	**36**	–	–
ANLG BLNK	–	–	–	–	–	32	–	**4**	–
GROUND (NOTE 2)	1,2,3,4	3,4,10	8,9,10,11,	1,2,13, 16,17,28	2,20,22,25, 27,45,47	1,2,3, 25,27,47	45,46,47, 48,49,50	11,12	–
CONTROL GATE	–	–	–	5,20	–	**26**	–	–	–
D6	–	–	–	–	35	–	22	–	–
D7	–	–	–	–	10	–	23	–	–
D8	–	–	–	–	36	–	24	–	–
D9	–	–	–	–	11	–	25	–	–
D10	–	–	–	–	37	–	26	–	–
D11	–	–	–	–	12	–	27	–	–
D12	–	–	–	–	38	–	28	–	–
D13	–	–	–	–	13	–	29	–	–
D14	–	–	–	–	39	–	30	–	–
D15	–	–	–	–	14	–	31	–	–
DGTL X	–	–	–	–	**29**	43	–	–	–
DGTL Y	–	–	–	–	**4**	18	–	–	–
DSPL CHAR	–	–	–	–	30	–	**12**	–	–
DSPL TRACE	–	–	–	–	31	–	**13**	–	–
FOCUS	–	9	–	**4,19**	–	–	–	–	–
FOCUS GATE	–	–	–	6,21	–	**34**	–	–	–
GRAT EN	–	–	–	–	–	36	**34**	–	–
HC GND▽$_5$	–	–	5	15,30	–	–	–	–	1
IN SEL A	–	–	–	–	16	–	**39**	–	–
IN SEL B	–	–	–	–	42	–	**40**	–	–
INTEN	11	–	–	–	–	**11**	–	–	–
L DGTL AVG	**10**	–	–	–	–	–	9	–	–
L DGTL BLNK	–	–	–	–	–	7	20	–	–
L INP–B–A	13	–	–	–	–	–	10	–	–
L INTEN MOD	–	–	–	–	–	37	32	–	–
LMANUAL	–	–	–	–	–	–	11	6	–
L MAX HOLD A	**12**	–	–	–	–	–	1	–	–
L MAX HOLD B	**14**	–	–	–	–	–	3	–	–
LNOISE	–	–	–	–	**19**	–	43	–	–
L PLOT GRAT	**16**	–	–	–	–	–	2	–	–
L PLOT TRACE	**18**	–	–	–	–	–	4	–	–
L STORE BLNK A	**20**	–	–	–	–	–	5	–	–
L STORE BLNK B	**19**	–	–	–	–	–	6	–	–
L SWP LIMIT	–	–	–	–	–	–	42	**5**	–
L SWP TRIG	–	–	–	–	–	–	60	**9**	–
L WRITE A	**17**	–	–	–		–	7	–	–
L WRITE B	**15**	–	–	–	–	–	8	–	–
L X CLAMP R	–	–	–	–	6	–	**14**	–	–
REQ CONV	–	–	–	–	17	–	**41**	–	–
RETRACE	–	–	–	–	–	–	57	**10**	–
SCALE INTEN	8	–	–	–	–	**9**	–	–	–
SLOW SWP	–	–	–	–	–	–	59	**7**	–
STORAGE OFF	–	–	–	–	–	–	58	**8**	–
STROKE BLNK	–	–	–	–	32	–	**15**	–	–
STRK BLNK LCHD	–	–	–	–	**7**	–	16	–	–
STRK DATA STRB	–	–	–	–	33	–	**17**	–	–
STRK GEN TIMG	–	–	–	–	8	–	**18**	–	–
STROKE LEN	–	–	–	–	**5**	35	–	–	–
STROKE SEL	–	–	–	–	34	–	**19**	–	–
SWEEP	–	–	–	–	44	42	–	**14**	–
VIDEO	–	–	–	–	50	50	–	**13**	–
X HOLD LEFT	–	–	–	–	9	–	**21**	–	–
X POSN 1	–	6	–	–	–	**39**	–	–	–
X POSN 2	–	5	–	–	–	**38**	–	–	–
Y POSN	–	11	–	–	–	**41**	–	–	–
Z MOD	6	–	–	–	–	**8**	–	–	–

Figure 8-50. Motherboard Assembly, Continuity Chart

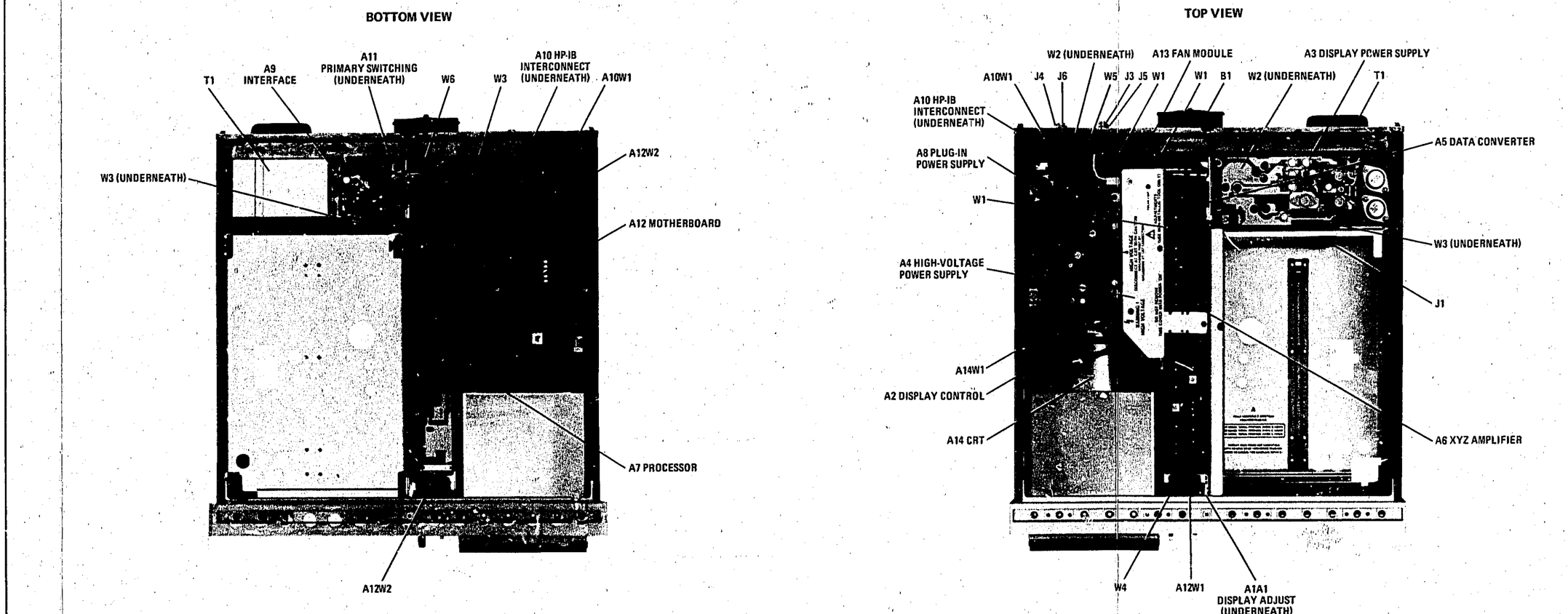


Figure 8-51. Major Assemblies, Components Locations

MANUAL CHANGES

MANUAL CHANGES

MANUAL IDENTIFICATION
Model Number: 853A
Date Printed: August 1982
Part Number: 00853-90001

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement:

Make all ERRATA corrections

Make all appropriate serial number related changes indicated in the tables below.

Serial Prefix or Number	Make Manual Changes
► 2244A	1

Serial Prefix or Number	Make Manual Changes

► NEW ITEM

NOTE

Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies quote the manual identification information from your supplement, or the model number and print date from the title page of the manual.

5 NOVEMBER 1982

2 Pages

HEWLETT PACKARD

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ERRATA

Page 2-1:
At end of page, change recommended fuse fo 220/240 Vac line voltage to 1.25A FAST BLO.

Table 6-3:
Change A3C1 to HP Part Number 0160-5214, Check Digit 8, CAPACITOR-FXD .1UF +-20% 500VDC CER.
Change A3C2 to HP Part Number 0160-3456, Check Digit 6, CAPACITOR-FXD 100PF +-10% 1KVDC CER.
Change A3MP6 to HP Part Number 0340-0949, Check Digit 8, TRANSISTOR INSULATOR.
Change F1 from HP Part Number 2110-0001 to 2110-0094, Check Digit 9, FUSE 1.25A 250V.

Figure 6-3:
Change item 8 to HP Part Number 0515-0395, Check Digit 9, SCREW-MACH M4 X 0.7 6MM-LG 90-DEG-FLH-HD.
Change item 20 to HP Part Number 0515-0413, Check Digit 2, (2 places) SCREW-MACH 6PCH PAN HD POZI DRIVE.

Figure 6-5:
Add mechanical parts:
Item 24, HP Part Number 0515-0412, Check Digit 1, SCREW-SMM3 25 PCH PAN-HD-PZ.
Item 25, HP Part Number 2190-0102, Check Digit 8, WASHER LK .472 ID.
Item 26, HP Part Number 2950-0035, Check Digit 8, NUT-HEX 15/32/32.
Position item 24 (2 places) at left side of Processor Assembly.
Positions items 25 (2 places) and 26 (2 places) at upper corners of rear panel.

Figure 6-6:
Add item 21, HP Part Number 2360-0135, Check Digit 8, (2 places) SCREW-MACH 632 1.500 IN-LG PAN-HD-POZI.
Add item 22, HP Part Number 2190-0018, Check Digit 5, (6 places) WASHER LK .141 ID.
Change number of item 15 to 4 places.
Three screws and lock washers attach each rear foot to the rear panel. Items 21 and 15 are the center and outer screws, respectively. Item 22 is the lock washer.

Figure 6-7:
Change item 11 to HP Part Number 2360-0117, Check Digit 5, SCREW-MACH 6-32 .375 PAN-HD-POZI.
Change item 13 to HP Part Number 5061-0089, Check Digit 0, KIT, FRONT HANDLES.

Figure 8-12 (1 of 2):
Change value of F1 for 220V, 240V operation to 1.25A.

Page 8-64:
In Counter circuit description, sixth paragraph, CPU address is $13 when ANLG FST SWP EN is high.

CHANGE 1

Table 6-3:
Change A4A1 to HP Part Number 08569-60080, Check Digit 0, HIGH VOLTAGE TRANSFORMER.
Change A4J2 to HP Part Number 1251-4647, Check Digit 3, CONNECTOR POST PP HDR.
Change A4J3 to HP Part Number 1251-4646, Check Digit 2, CONNECTOR POST TP HDR.
Change A4R28 to HP Part Number 0699-0171, Check Digit 7, RESISTOR 6.5M 5% 1W C TC=0+-100.
Change A4R29 to HP Part Number 2100-3359, Check Digit 4, RESISTOR-TRMR 2M 20% C

SIDE-ADJ 1-TRN.
Change A4R30 to HP Part Number 0699-0519, Check Digit 7, RESISTOR 12M 5% 1W.

Pages 8-27 through 8-29:
In circuit description, change cathode and filament voltage to -2350V, and control grid to -2400V.

Figure 8-14:
In function block H, change value of R28 to 6.5M, R29 to 2M, and R30 to 12M.
Change cathode and filament voltage to -2350V, and control grid to -2400V.
Change A4A1 part number to 08569-60080.